MECL

INTEGRATED CIRCUITS
MC300/MC350 SERIES

MECL

MC300 SERIES

INDEX

FUNCTIONS AND CHARACTERISTICS

V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C

Function	Type (1)	DC Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Case
GATES					
5-Input OR/NOR Gate	MC301	25	7.5	37	602B,606
3-Input OR/NOR Gate	MC306	↓	7.5	37	↓
3-Input OR/NOR Gate	MC307		7.5	15	
Dual 2-Input NOR Gate	MC309		7.0	54	
Dual 2-Input NOR Gate	MC310		7.0	54	
Dual 2-Input NOR Gate	MC311		7.0	41	
Dual 3-Input NOR Gate (With Internal Bias)	MC312A		7.5	70	
Quad 2-Input NOR Gate	MC313F	↓	7.0	125	607
FLIP-FLOPS					
R-S Flip-Flop	MC302	25	11	42	602B,606
AC-Coupled J-K Flip-Flop	MC308	↓	8.5	87	↓
AC-Coupled J-K Flip-Flop	MC314		12	118	
HALF-ADDER					
Half-Adder	MC303	25	7.5	63	602B,606
GATE EXPANDER					
5-Input Gate Expander	MC305	—	4.5	—	602B,606
DRIVERS					
Bias Driver	MC304	25	—	18	602B,606
Line Driver	MC315	—	14	180 (2)	↓
Lamp Driver	MC316	—	—	135	
TRANSLATORS					
Level Translator — MECL to Saturated Logic	MC317	7 (DTL)	27.5	63	602B,606
Level Translator — Saturated Logic to MECL	MC318	25 (MECL)	17	105	602B,606

(1) G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC301G = Metal Can, MC301F = Flat Package.)

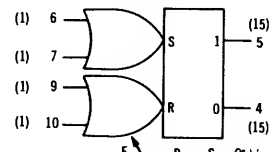
(2) With 93-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC300 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC304, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are included in this section of the Data Book.

MC302 — R-S FLIP-FLOP

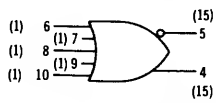


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

t_{dr} = 10.5 ns
P_D = 42 mW

DC Set-Reset flip-flop with expandable input and buffered outputs.

MC301 — 5-INPUT GATE



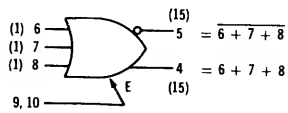
$5 = \overline{6 + 7 + 8 + 9 + 10}$

$4 = 6 + 7 + 8 + 9 + 10$

t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC306 — 3-INPUT GATE



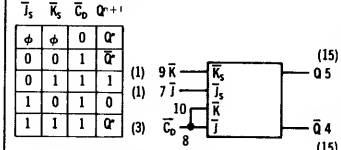
t_{dl} = 6.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC308 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

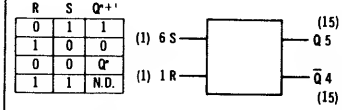
$\overline{J}_s$	$\overline{K}_s$	$\overline{C}_D$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}_s$ and $\overline{K}_s$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}_s$ and $\overline{K}_s$ inputs would be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

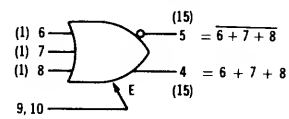
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC307 — 3-INPUT GATE



t_{dl} = 6.0 ns
P_D = 15 mW

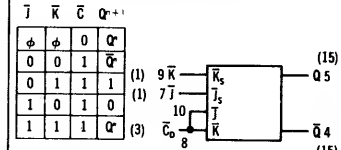
*No pull-down resistors

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC306, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on the data sheet).

MC314 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

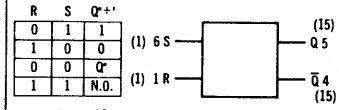
$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

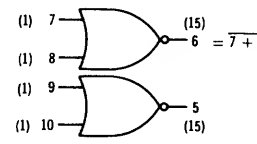
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

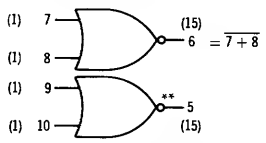
MC309 — DUAL 2-INPUT GATE



t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

MC310 — DUAL 2-INPUT GATE

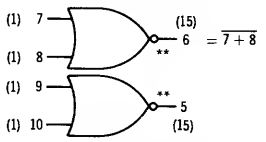


**Optional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

t_{dl} = 6.5 ns P_D = 27 mW/gate

Provides the positive logic "NDR" function. Same as MC3D9 with one output pull-down resistor optional (see schematic diagram on the data sheet).

MC311 — DUAL 2-INPUT GATE

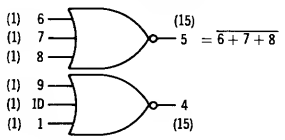


**Optional pull-down resistor If resistor is desired, connect pin 4 to pin 5 or pin 6.

t_{dl} = 6.5 ns P_D = 21 mW/gate

Provides the positive logic "NDR" function. Same as MC309 with one output pull-down resistor omitted and the second optional (see schematic diagram on the data sheet).

MC312A — DUAL 3-INPUT GATE

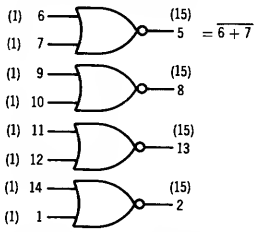


t_{dl} = 6.5 ns

P_D = 35 mW/gate

Provides the positive logic "NDR" function, and features an internal bias driver. This gate without the bias driver is available as the MC312.

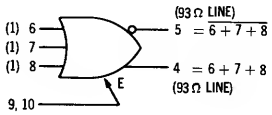
MC313F — QUAD 2-INPUT GATE



t_{dl} = 6.5 ns P_D = 31 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC315 — LINE DRIVER

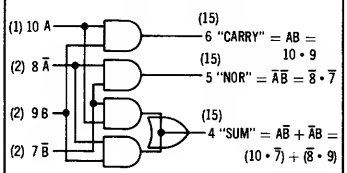


t_{dl} = 14 ns

P_D = 180 mW (with 93 Ω load)

Drives lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC303 — HALF-ADDER

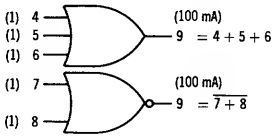


t_{dl} = 7 ns

P_D = 63 mW

Provides the "SUM", "CARRY", and "NOR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

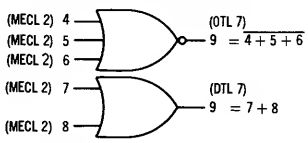
MC316 — LAMP DRIVER



P_D = 135 mW

Capable of driving 6-volt lamps. Positive "NOR" function is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC317 — LEVEL TRANSLATOR

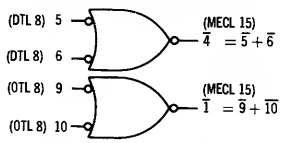


t_{dr} = 30 ns

P_D = 63 mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NOR" function is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "OR" is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC318 — LEVEL TRANSLATOR

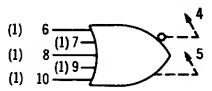


t_{dl} = 17 ns

P_D = 105 mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying OTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC305 — 5-INPUT EXPANDER



t_{dl} = 5 ns

For use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

Note:

Any unused input should be connected to V_{EE}.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

"0" = −1.55 V
"1" = −0.75 V
} typical

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

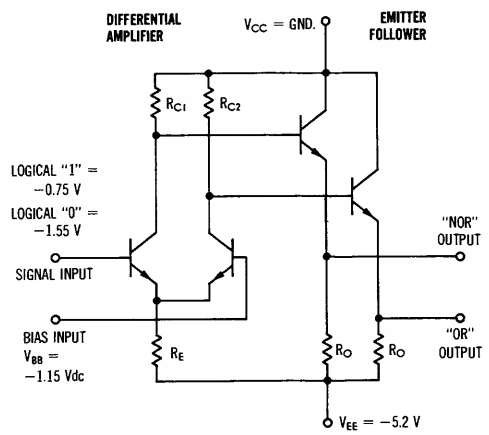
A bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE}-drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE}-drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC304. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V

FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

DEFINITIONS

e_{in} AC signal applied to the input

e_{out} AC signal at the output

I_C Amount of current drawn from the positive power supply by the test unit

I_{CEX} Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential

I_E Amount of current drawn from the test unit by the negative power supply

I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input

I_L Current drawn from a node when that node is at ground potential

t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge

t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge

t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge

t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge

t_f Time required for the output pulse to go more negative from its 90% point to its 10% point

t_r Time required for the output pulse to go more positive from its 10% point to its 90% point

V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input

V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input

V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero

V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input

V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input

V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity

V_H Logical "1" input voltage

V_L Logical "0" input voltage

V_{OH} High-level output voltage when the saturated logic circuit output is in an "off" condition

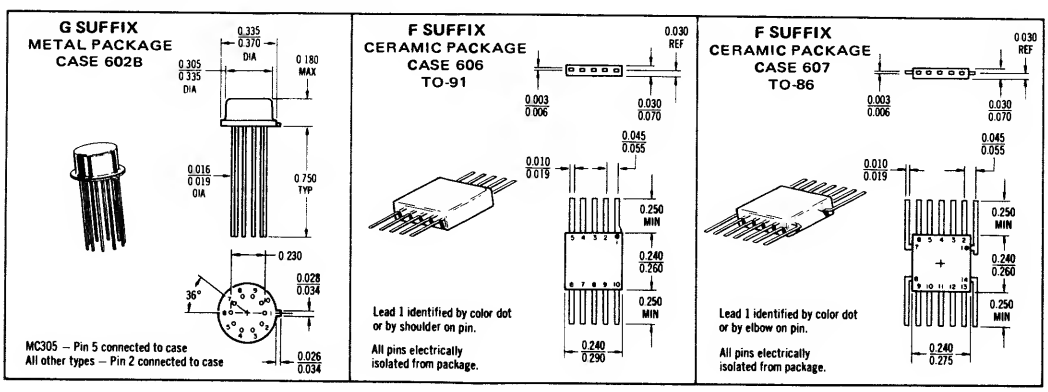
V_{OL} Low-level output voltage when the saturated logic output circuit is in an "on" condition

ΔV_1, ΔV_5 Change in the "1" level output voltage as the load is varied from no load to full load

PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

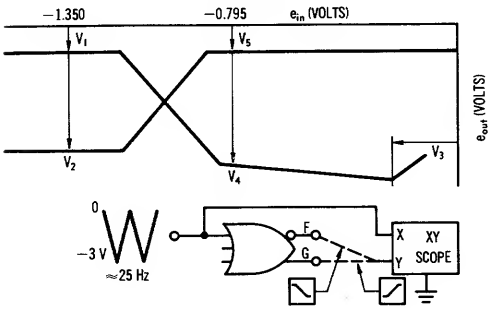
Exception: Type MC313F is available only in the TO-86 14-lead flat package.

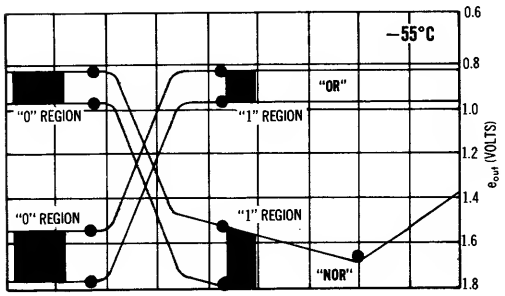


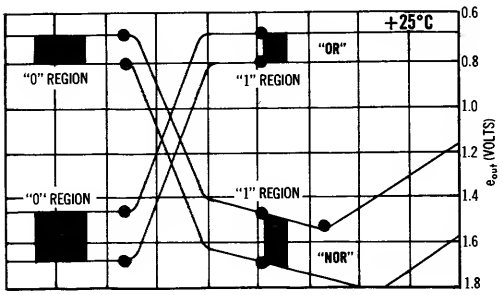
WORST-CASE TRANSFER CHARACTERISTICS

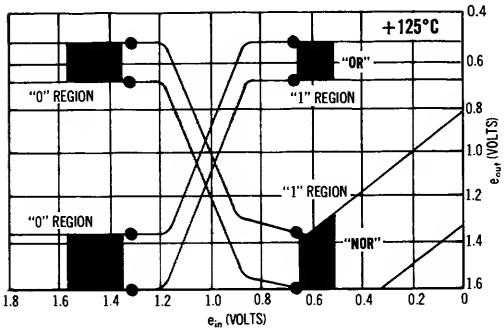
The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS









MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0 Vdc)	V_{EE}	−10	Vdc
Base Input Voltage (V_{CC} = 0 Vdc)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	−55 to +125	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

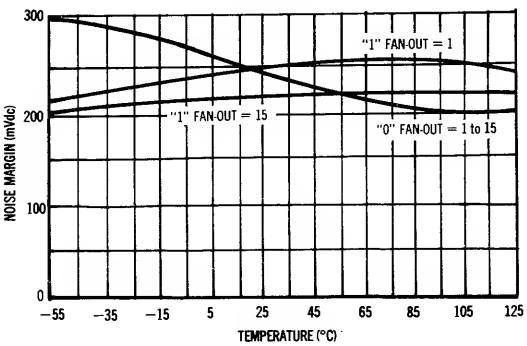
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

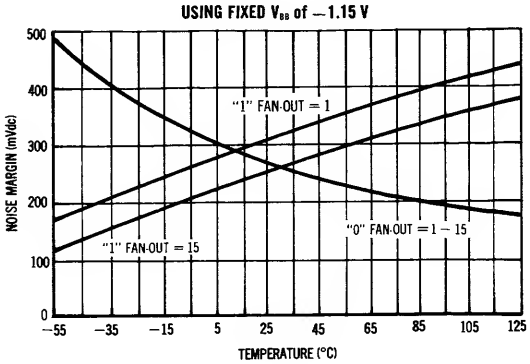
The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC304 bias driver, as compared with non-compensated fixed bias source, bottom.

Note: Any unused input should be connected to V_{EE}.

USING MC304



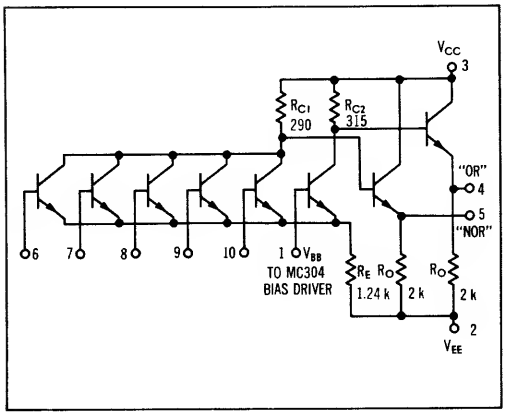
USING FIXED V_{BB} of −1.15 V



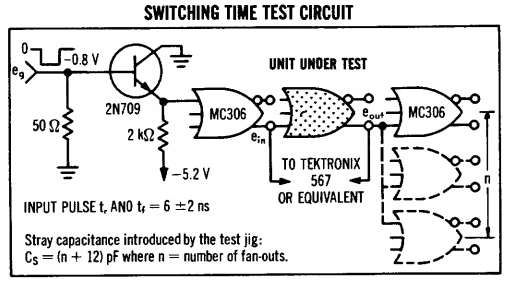
5-INPUT GATE

MC301

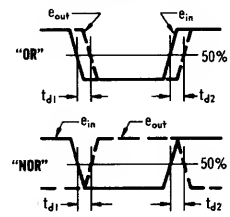
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



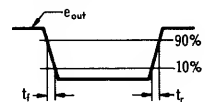
SWITCHING TIME TEST CIRCUIT



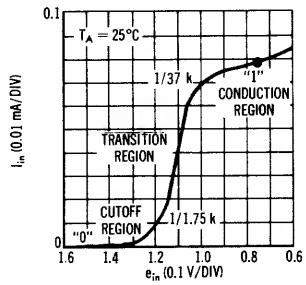
PROPAGATION DELAY



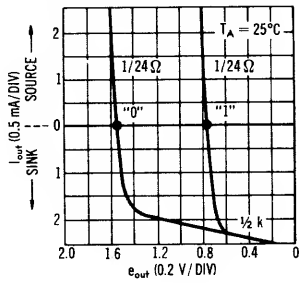
RISE AND FALL TIME



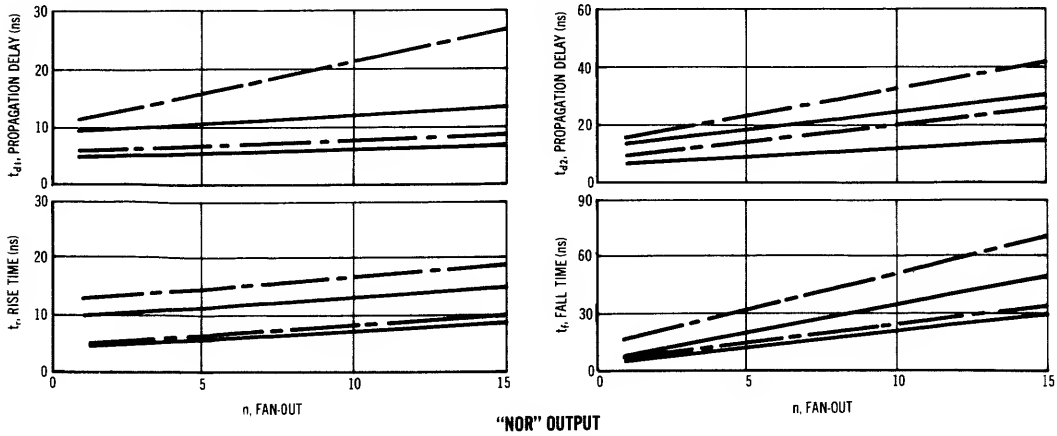
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" OUTPUT

——— −55°C and +25°C

— — — +125°C

ELECTRICAL CHARACTERISTICS

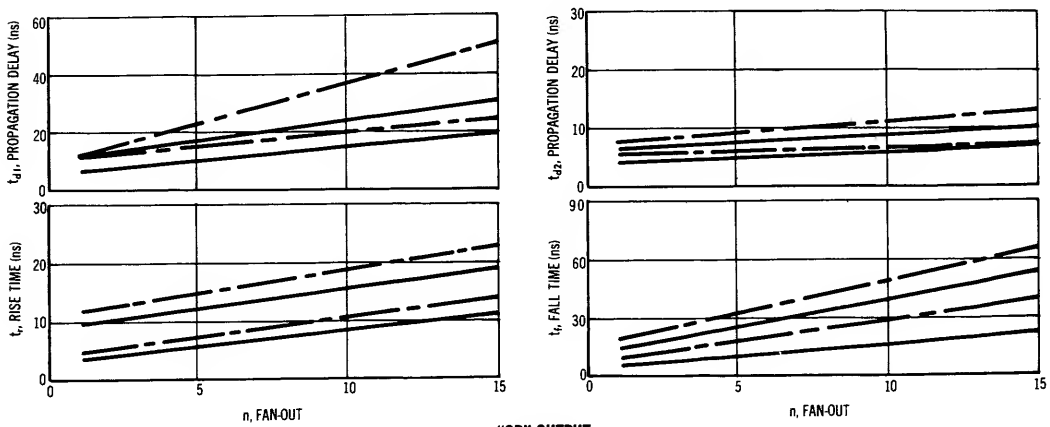
@ Test Temperature	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	8.85	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_4 (5)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_2 (4)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4②	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9	1	10①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	8.0	12.0	8.5	12.5	10.0	15.5	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	6.5	10.0	6.5	11.0	7.5	14.0	↓
	6	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	5.5	9.0	6.0	10.0	8.0	12.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	7.5	11.0	8.0	12.5	10.0	15.5	
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	6.5	9.0	7.0	10.0	10.5	15.5	
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	8.5	14.0	9.0	14.5	11.0	17.5	
Fall Time	6	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	7.0	11.5	7.5	13.0	10.0	16.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	7.0	12.0	7.5	12.5	10.0	15.5	↓

Pins not listed are left open

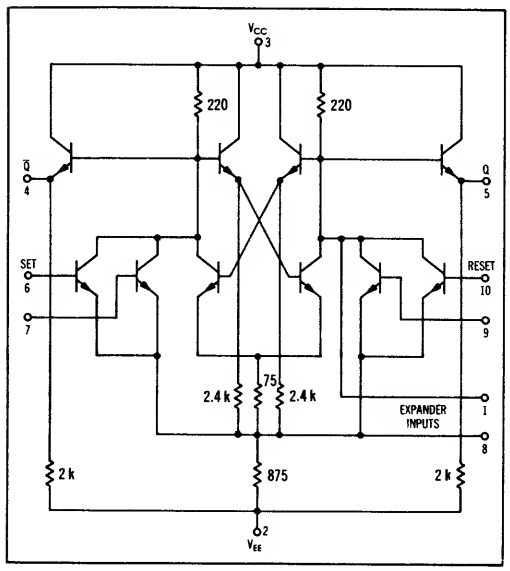
① Input voltage is adjusted to obtain dV "NOR / dV_{in} = "0".

② Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

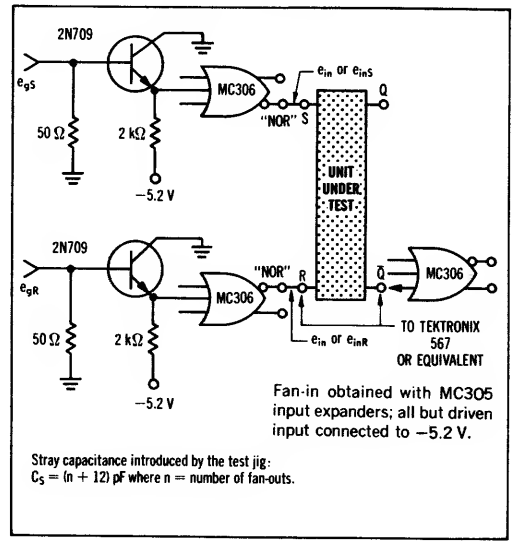


MC302

DC Set-Reset flip-flop with an expandable input and buffered outputs.



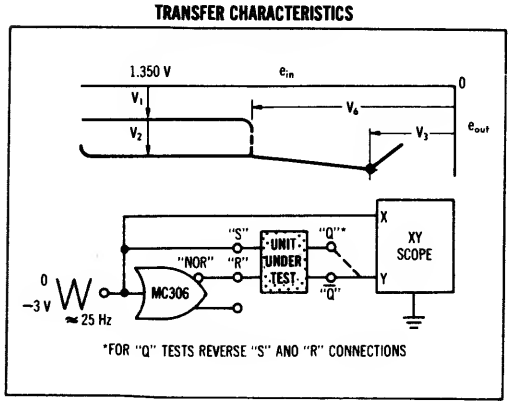
SWITCHING TIME TEST CIRCUIT



Fan-in obtained with MC305 input expanders; all but driven input connected to −5.2 V.

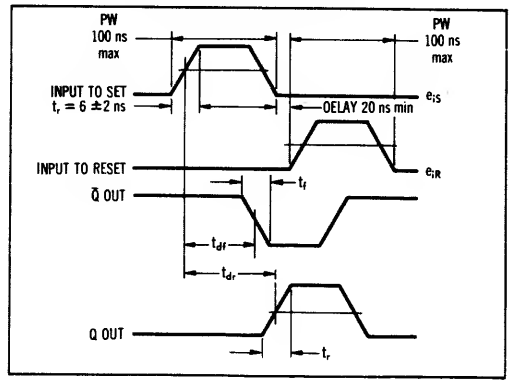
Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

SWITCHING TIME WAVEFORMS



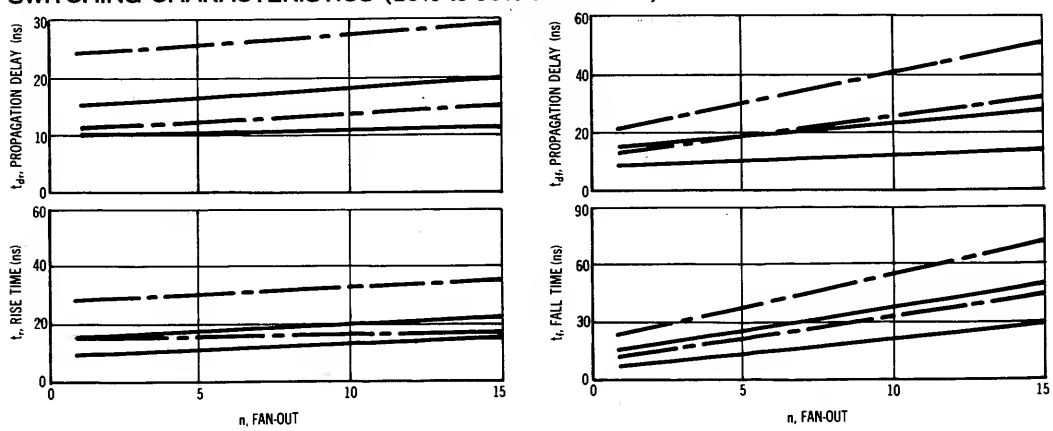
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_E (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	9③	2,6,7,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10③	2,6,7,9	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	2,7,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7③	2,6,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5④	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4③	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,9	6,10②	—	3	V_4 (6,10)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
Switching Times	Pulse In	Pulse Out							**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	9.0	14.0	10.5	16.0	22.0	29.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	8.5	14.0	11.5	19.5	16.0	24.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	9.0	15.0	11.5	19.0	23.0	31.0	
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	7.0	13.0	12.5	19.5	18.0	29.0	

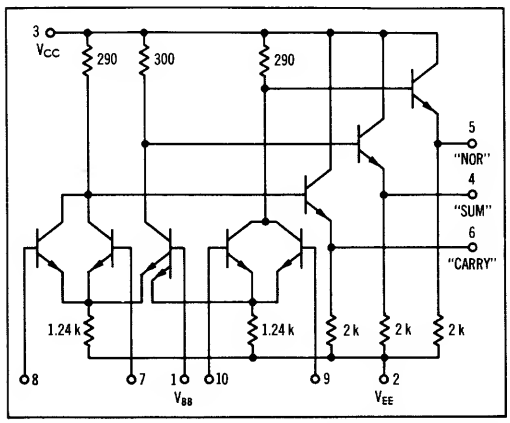
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV\ "\overline{Q}"/dV_{in} = 0$; $dV\ "Q"/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
④ Apply momentary $V_{I\,max}$ to set output, then V_L for measurement. ② Input voltage is adjusted to obtain $dV_1/dV_{in} \approx \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

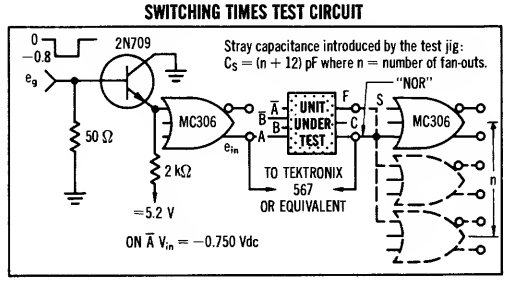


MC303

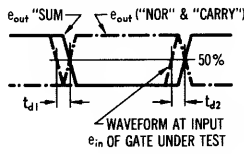
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



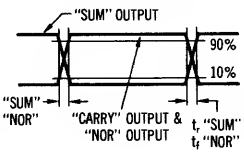
SWITCHING TIMES TEST CIRCUIT



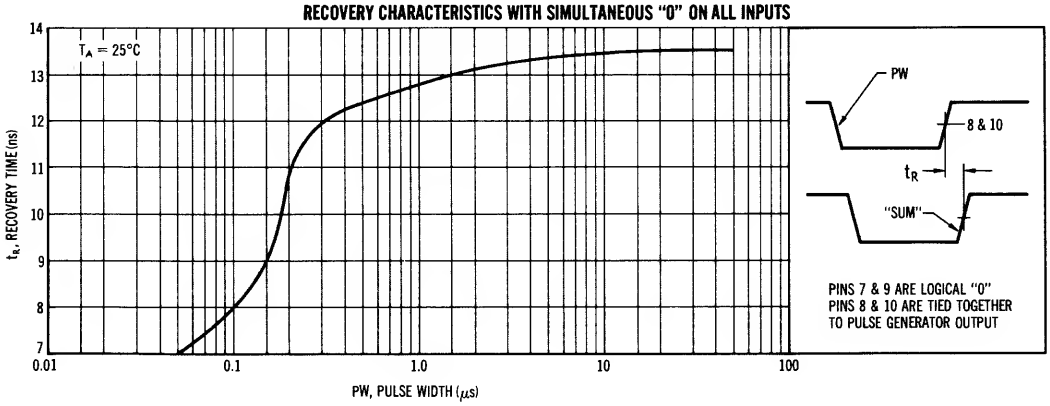
PROPAGATION DELAY



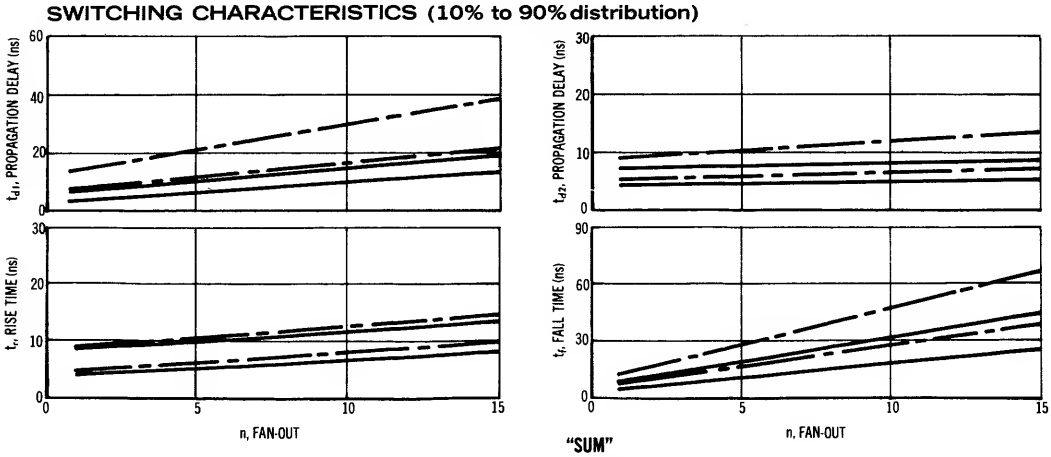
RISE AND FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



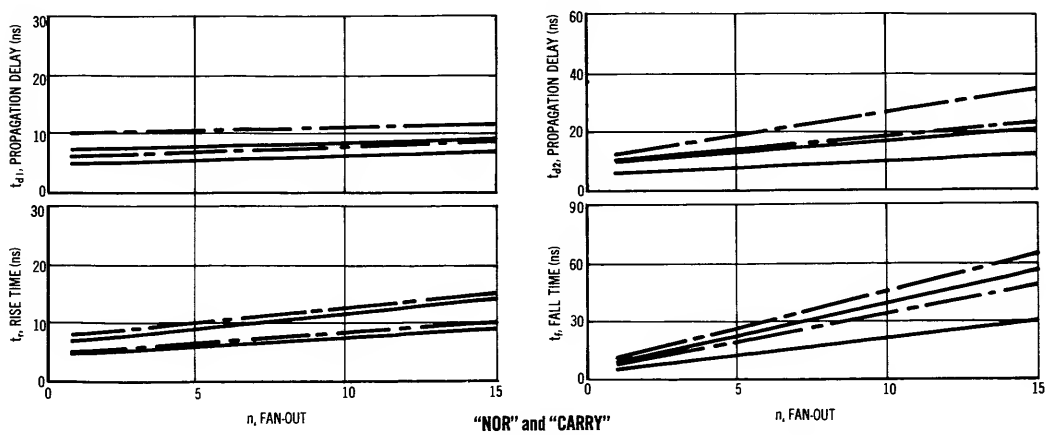
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
−55°C	—	−0.945	−1.450	−5.20	−1.25
+25°C	−0.690	−0.795	−1.350	−5.20	−1.15
+125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{l\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.3	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)							
	—	10	7	2,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6②	3	$\triangle V_1$ (6)	—	−0.055	—	−0.055	—	−0.060	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4②	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.65	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.40	—	−0.55	—	−0.65	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.0	10.0	6.0	11.0	7.5	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.0	10.0	6.0	11.0	7.5	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.0	12.0	8.0	12.0	10.5	17.0	
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	7.5	10.5	7.5	11.0	10.0	15.0	
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	7.5	10.5	7.5	11.0	10.0	15.0	
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	5.5	8.0	5.5	8.5	7.5	12.0	
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	6.0	11.5	6.5	12.0	7.5	14.0	
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	6.0	11.5	6.5	12.0	7.5	14.0	
	—	7	—	2,8,9	1	10	4	3	t_r (4)	6.0	10.0	6.5	11.0	10.0	16.0	
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	7.5	12.0	8.0	13.5	10.5	16.5	
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	7.5	12.0	8.0	13.5	10.5	16.5	
	—	7	—	2,8,9	1	10	4	3	t_f (4)	8.0	12.5	8.5	13.5	11.0	18.0	

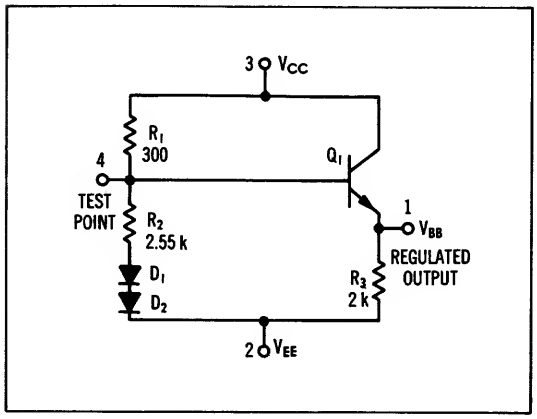
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{"NOR"}/dV_{in} = 0$ or $dV_{"CARRY"}/dV_{in} = 0$.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC304

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ± 1%
@ Test Temperature	−55°C	−5.20
	+25°C	−5.20
	+125°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	2	—	3	I_E(2)	—	4.4	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.19	−1.32	−1.09	−1.22	−0.95	−1.08	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of −55 to +125°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

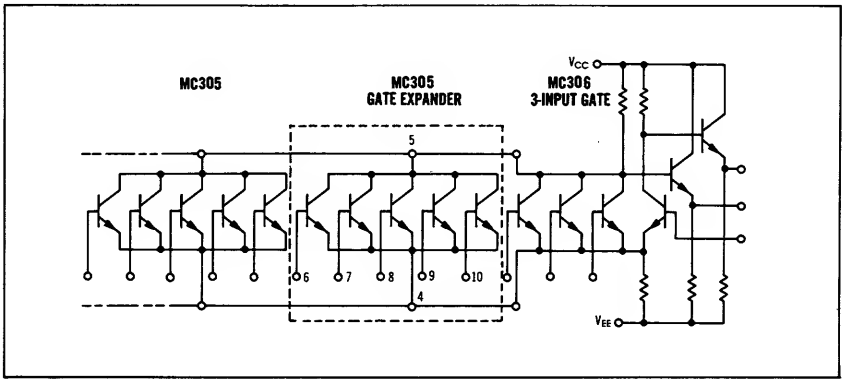
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

$V_{BB} = -1.15$ nominal output voltage at 25°C

MC305

A 5-input expander for use with the MC302, MC306, MC307, and MC315. Each expander unit increases the fan-in of the basic gate by five.



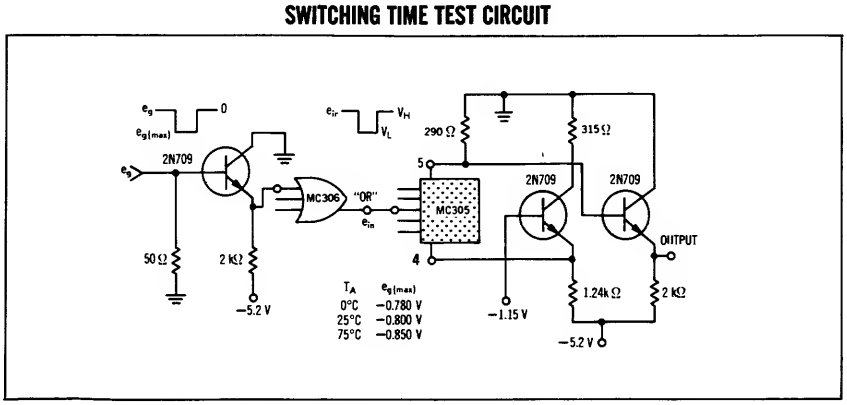
ELECTRICAL CHARACTERISTICS

		Test Conditions					
		Vdc ±1%					mAdc
@ Test Temperature	−55°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
	+25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
	+125°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CB} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	μAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—	↓	—	↓	—	↓	↓
	4	9	—	—	—	—	5	I_{BL} (9)	—	↓	—	↓	—	↓	↓
	4	10	—	—	—	—	5	I_{BL} (10)	—	↓	—	↓	—	↓	↓
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	100.0	μAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	−0.810	−0.880	−0.680	−0.730	−0.490	−0.540	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	9	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	10	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	①	—	—	—	—	—	—	t_{d1} 5.0	8.0	5.0	8.5	5.5	9.5	ns
	8	①	—	—	—	—	—	—	t_{d2} 4.0	8.0	4.0	8.0	4.5	10.0	↓
Rise Time	8	①	—	—	—	—	—	—	t_r 8.0	10.5	8.5	11.5	6.5	13.0	↓
Fall Time	8	①	—	—	—	—	—	—	t_f 3.0	8.5	3.5	8.5	4.5	9.5	↓

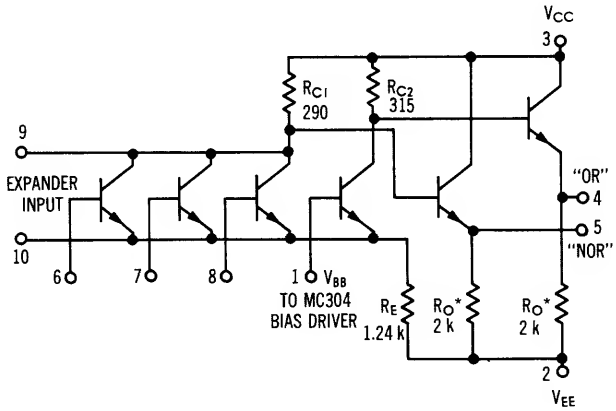
Pins not listed are left open. ①See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



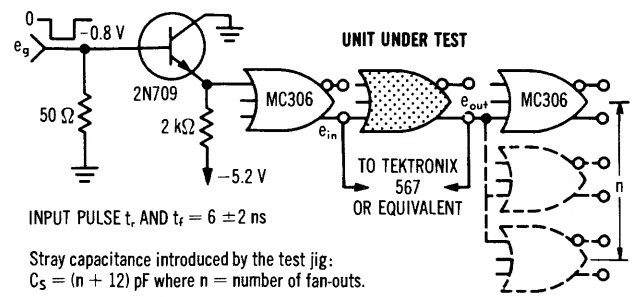
MC306 · MC307

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC307 omits output pull-down resistors, permitting reduction of power dissipation.



*Resistors R_O are omitted in MC307 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

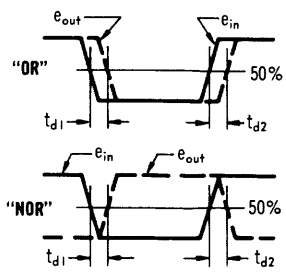
SWITCHING TIME TEST CIRCUIT



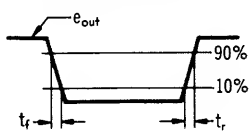
INPUT PULSE t_r AND t_f = 6 ±2 ns

Stray capacitance introduced by the test jig:
C_S = (n + 12) pF where n = number of fan-outs.

PROPAGATION DELAY

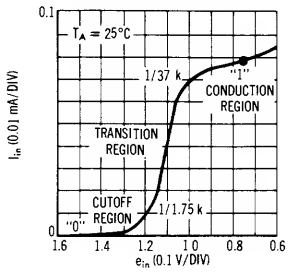


RISE AND FALL TIME

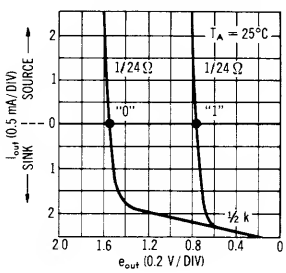


Fan-in obtained with MC305 input expanders; all but driven input connected to −5.2 V.

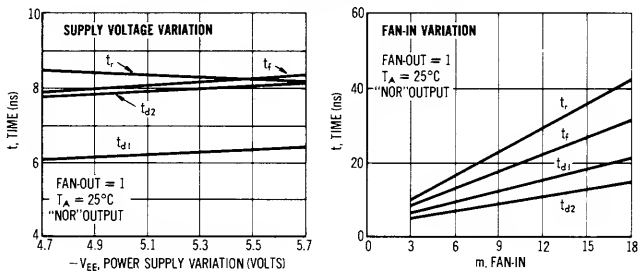
TYPICAL INPUT CHARACTERISTICS



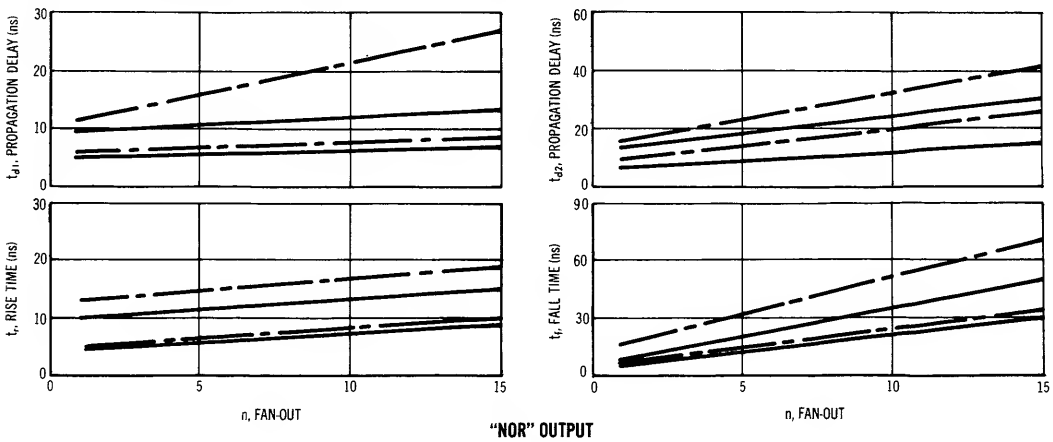
TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SWITCHING TIME VARIATIONS MC306



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" OUTPUT

—— —55°C and +25°C

— — +125°C

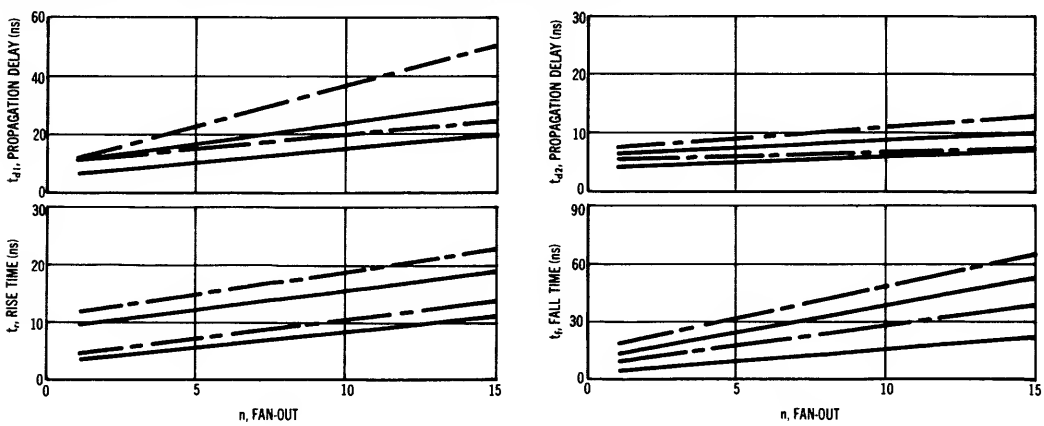
ELECTRICAL CHARACTERISTICS

Test Conditions Vdc ±1%					
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply MC306	—	—	—	2,6,7,6	1	—	—	3	I_E (2)	—	6.65	—	6.65	—	6.15	mAdc
Drain Current MC307	—	—	—	2,6,7,6	1	—	—	3	I_E (2)	—	3.6	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,6	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	6	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,6	1	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	2,6,6	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	6	2,6,7	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,6	1	—	—	3	V_4 (5)	−1.560	−1.650	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	2,6,6	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	6	—	2,6,7	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,6	1	—	—	3	V_5 (4)	−0.625	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	7	—	2,6,6	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	6	—	2,6,7	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,6	1	—	—	3	V_2 (4)	−1.560	−1.650	−1.465	−1.750	−1.340	−1.675	Vdc
	—	—	7	2,6,6	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,6	1	—	5②	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,6	1	—	4②	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,6	1	6①	—	3	V_2 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	2,6,6	1	7①	—	3	V_2 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_2 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8	1	—	—	3	t_{d1} (4)	7.0	11.0	7.0	11.5	9.5	14.5	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	5.5	10.0	5.5	10.5	7.0	12.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	5.5	10.0	5.5	11.0	7.0	12.5	
	6	5	—	2,7,6	1	—	—	3	t_{d2} (5)	7.0	10.5	7.0	11.0	9.5	14.5	
Rise Time	6	4	—	2,7,6	1	—	—	3	t_r (4)	6.0	6.5	6.0	10.0	6.0	13.0	
	6	5	—	2,7,6	1	—	—	3	t_r (5)	7.5	11.5	7.5	12.5	9.5	15.0	
Fall Time	8	4	—	2,7,6	1	—	—	3	t_f (4)	6.5	10.5	6.5	12.0	9.0	15.0	
	6	5	—	2,7,6	1	—	—	3	t_f (5)	6.5	12.0	6.5	12.5	9.0	15.0	↓

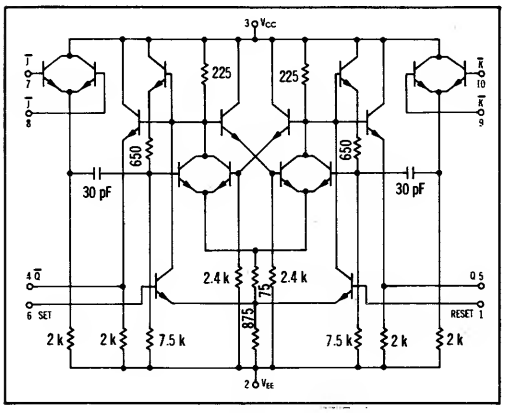
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR / dV_{in} = 0. ② Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC308

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS

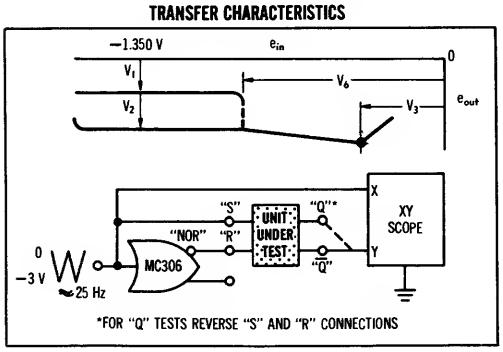


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

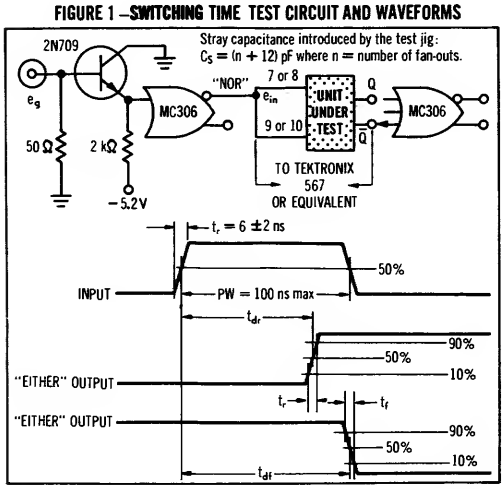


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

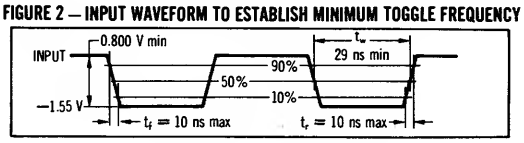


FIGURE 3 – SENSITIVITY (NO TOGGLE)

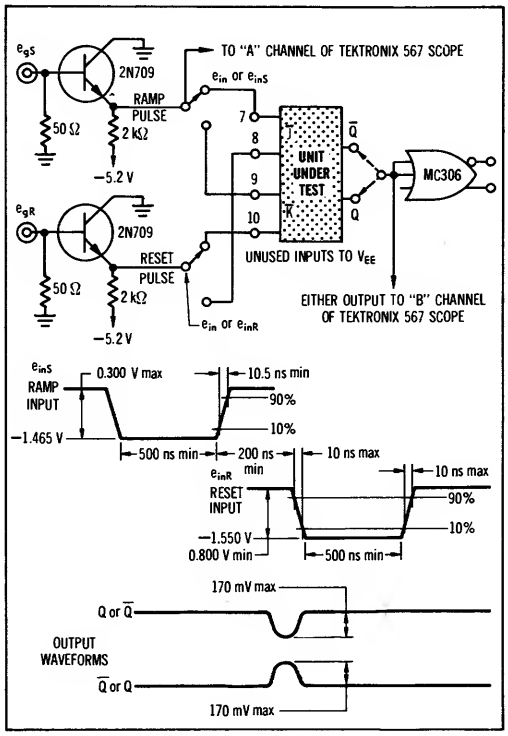
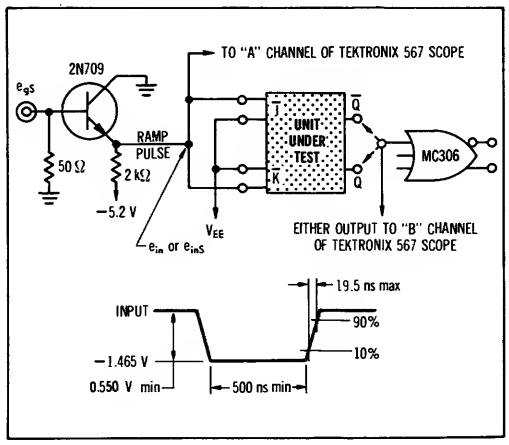


FIGURE 4 – SENSITIVITY (TOGGLE)



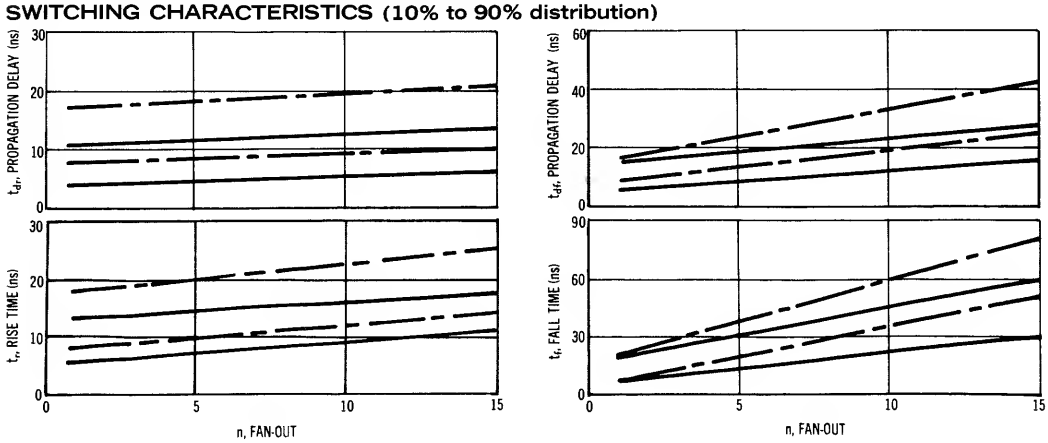
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5②	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\overline{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4②	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_6 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{req}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5		1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	7,10	4,5		1,2,6,8,9	—	—	3	t_{dr} (4,5)	7.0	11.5	7.0	12.5	9.5	18.5	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	8.5	14.0	8.5	14.5	10.0	16.5	↓
Rise Time	7,10	4,5		1,2,6,8,9	—	—	3	t_r (4,5)	6.5	13.0	6.5	13.0	10.0	18.5	
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	7.5	14.5	8.5	15.5	11.5	20.0	

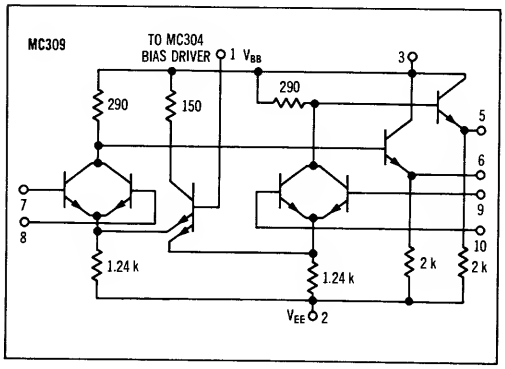
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{in}/dV_o = 0$. ② Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_I/dV_{in} = \infty$.

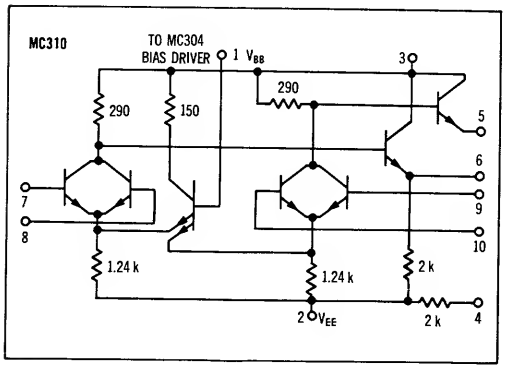
SWITCHING CHARACTERISTICS (10% to 90% distribution)

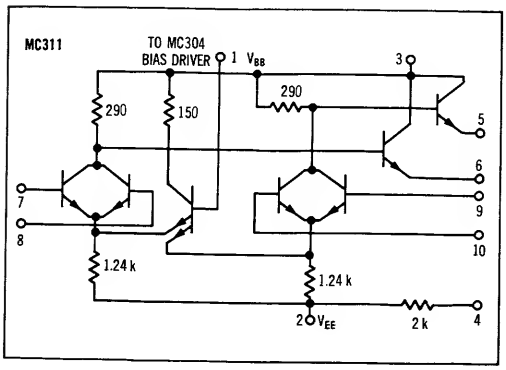


MC309 · MC310 · MC311

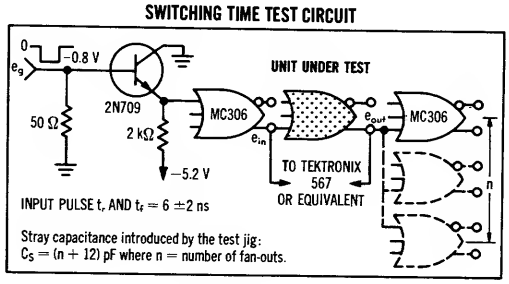
Dual 2-input gates that provide the positive logic "NOR" function. MC309 has two output pull-down resistors; MC310 has one of the output pull-down resistors optional; MC311 omits one output pull-down resistor and has the second optional.



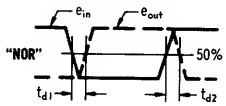




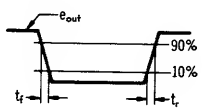
SWITCHING TIME TEST CIRCUIT



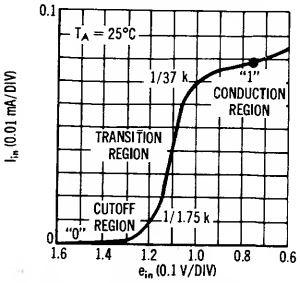
PROPAGATION DELAY



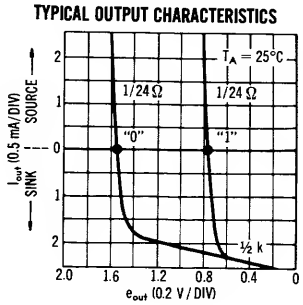
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



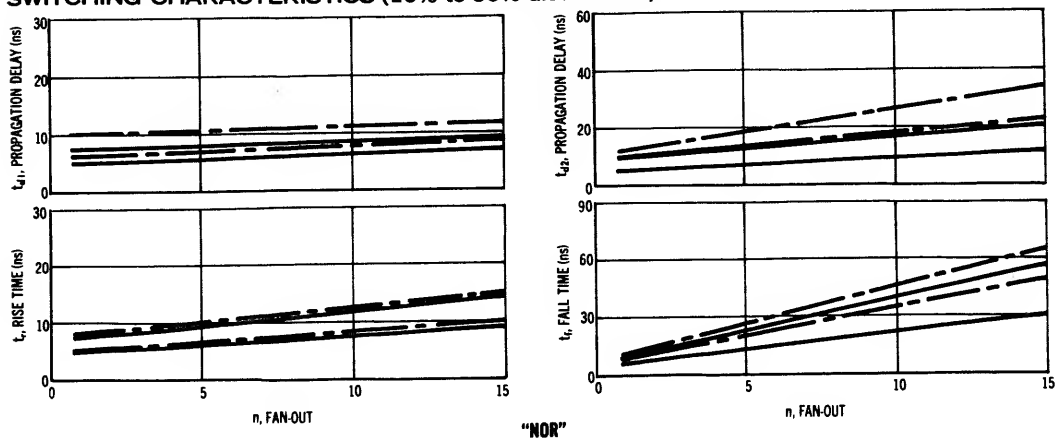
ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%				
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_{IH} Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply MC309, MC310	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.0	—	13.0	—	12.0	mAdc
Drain Current MC311	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	10.1	—	10.1	—	9.3	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1"	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
Output Voltage	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)							
"NOR" Logical "0"	—	7	—	2,8,9,10	1	—	—	3	V_0 (6)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
Output Voltage	—	8	—	2,7,9,10	1	—	—	3	V_0 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_0 (5)							
	—	10	—	2,7,8,9	1	—	—	3	V_0 (5)							
"NOR" Output Voltage Change	—	—	—	2,7,8,9,10	1	—	6④	3	ΔV_1 (6)	—	−0.055	—	−0.055	—	−0.060	Vdc
(No load to full load)	—	—	—	2,7,8,9,10	1	—	5④	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.060	Vdc
"NOR" Saturation	—	—	—	2,8,9,10	1	7①	—	3	V_S (6)	—	−0.40	—	−0.55	—	−0.68	Vdc
Breakpoint Voltage	—	—	—	2,7,9,10	1	8①	—	3	V_S (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_S (5)	—		—		—		
	—	—	—	2,7,8,9	1	10①	—	3	V_S (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	6	—	2,8,9,10	1	—	—	3	t_{d1} (6)	5.5	10.0	6.0	11.0	7.0	12.0	ns
	10	5	—	2,7,8,9	1	—	—	3	t_{d1} (5)	5.5	10.0	6.0	11.0	7.0	12.0	↓
	7	6	—	2,8,9,10	1	—	—	3	t_{d2} (6)	6.5	13.0	7.0	13.5	9.5	15.0	
	10	5	—	2,7,8,9	1	—	—	3	t_{d2} (5)	6.5	13.0	7.0	13.5	9.5	15.0	
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	6.0	12.0	6.0	12.0	7.0	13.5	
	10	5	—	2,7,8,9	1	—	—	3	t_r (5)	6.0	12.0	6.0	12.0	7.0	13.5	
Fall Time	7	6	—	2,8,9,10	1	—	—	3	t_f (6)	7.0	13.0	7.5	14.0	9.5	17.0	
	10	5	—	2,7,8,9	1	—	—	3	t_f (5)	7.0	13.0	7.5	14.0	9.5	17.0	↓

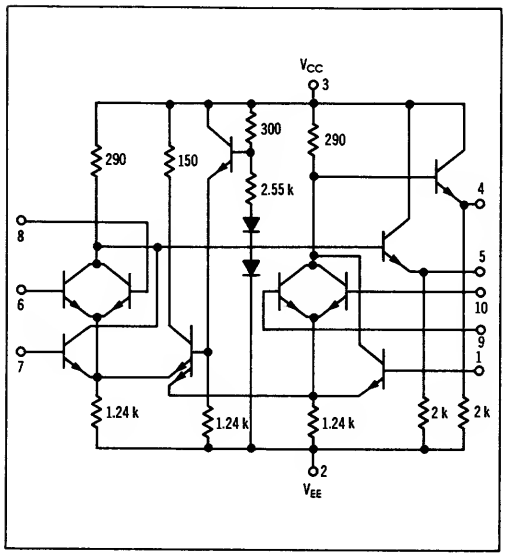
Pins not listed are left open For MC310, connect pin 4 to pin 5 for all tests ① Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$.
④ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

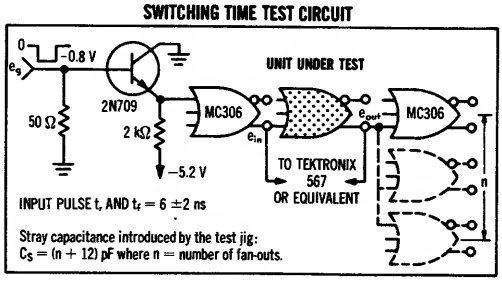


MC312A

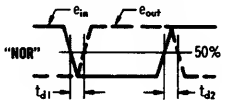
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC312.



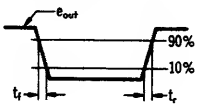
SWITCHING TIME TEST CIRCUIT



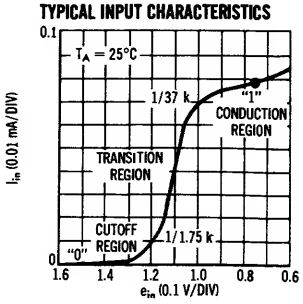
PROPAGATION DELAY



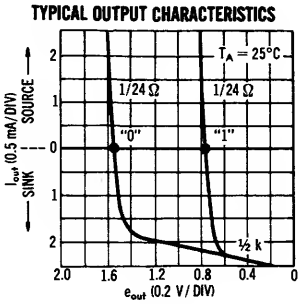
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



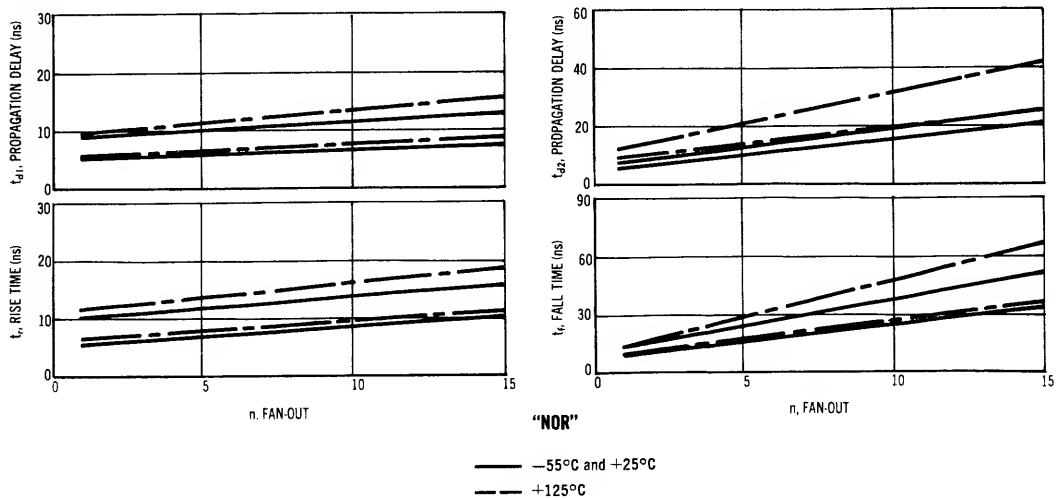
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5①	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	1	2,6,7,8,9,10	—	4③	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—	↓	—	↓	—	↓	
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

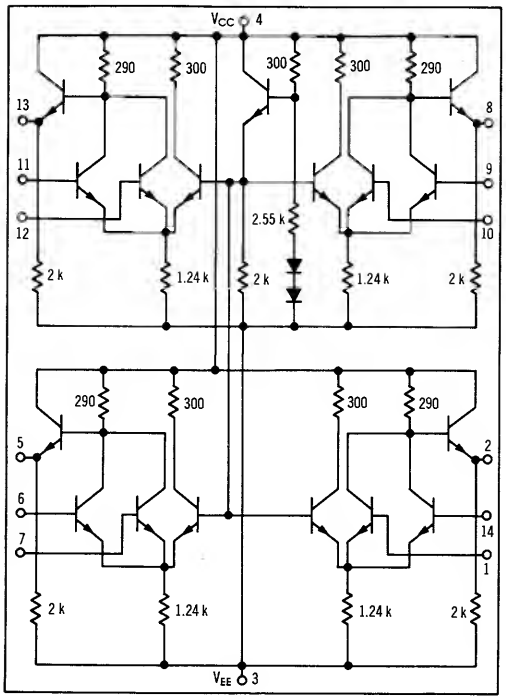
Pins not listed are left open.
①Input voltage is adjusted to obtain dv "NOR" / $dV_{in} = 0$. ③Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

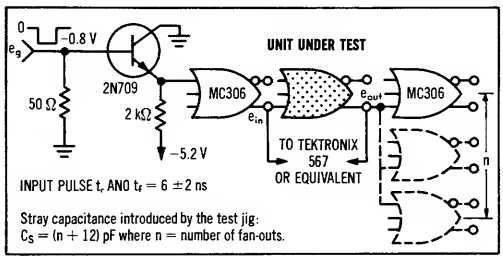


MC313F

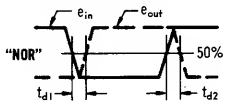
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



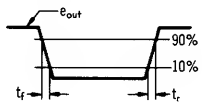
SWITCHING TIME TEST CIRCUIT



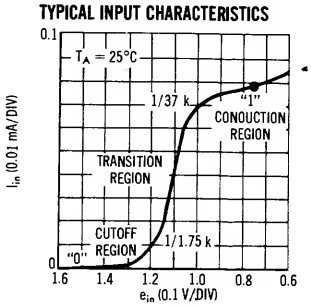
PROPAGATION DELAY



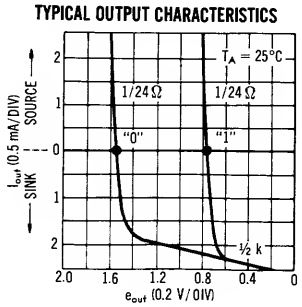
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



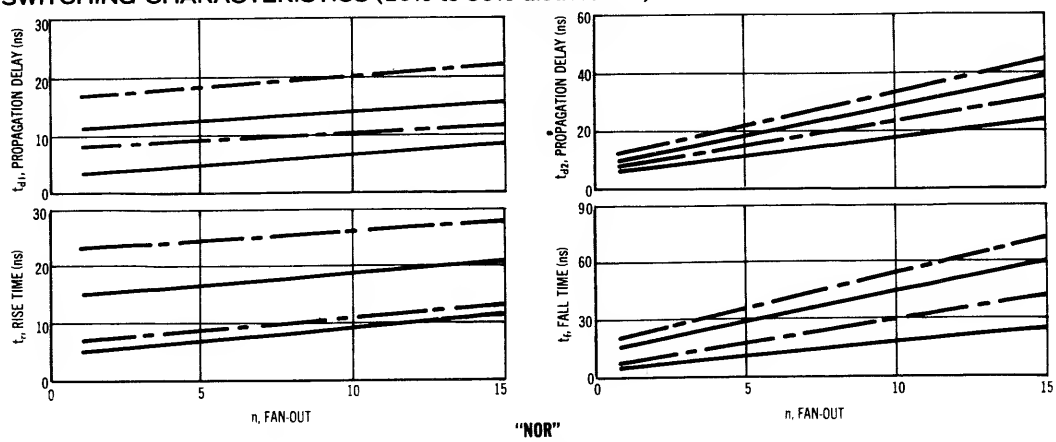
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	1,3,6,7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—	↓	—	—	↓
	11	—	—	1,3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—	↓	—	—	↓
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—	↓	—	—	↓
	14	—	—	1,3,6,7,9,10,11,12	—	—	4	I_{in} (14)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_1 (2)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_1 (8)	↓	↓	↓	↓	↓	↓	↓
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_1 (13)	↓	↓	↓	↓	↓	↓	↓
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_1 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	—	6	—	1,3,7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	1,3,6,7,10,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)	↓	↓	↓	↓	↓	↓	↓
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)	↓	↓	↓	↓	↓	↓	↓
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2②	4	$\triangle V_1$ (2)	—	−0.055	—	−0.055	—	−0.060	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5②	4	$\triangle V_1$ (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8②	4	$\triangle V_1$ (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	13②	4	$\triangle V_1$ (13)	—	↓	—	↓	—	↓	↓
"NOR" Saturation Breakpoint Voltage	—	—	—	1,3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	−0.40	—	−0.55	—	−0.68	Vdc
	—	—	—	1,3,6,7,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	10①	—	4	V_3 (8)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	12①	—	4	V_3 (13)	—	↓	—	↓	—	↓	↓
Switching Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d1} (8)	↓	↓	↓	↓	↓	↓	↓
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)	↓	↓	↓	↓	↓	↓	↓
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)	↓	↓	↓	↓	↓	↓	
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_r (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)	↓	↓	↓	↓	↓	↓	
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)	↓	↓	↓	↓	↓	↓	
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)	↓	↓	↓	↓	↓	↓	

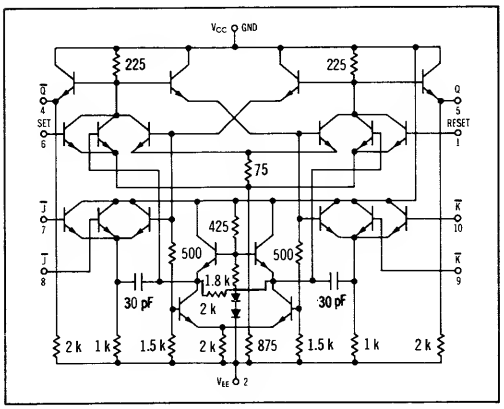
Pins not listed are left open ① Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$. ② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

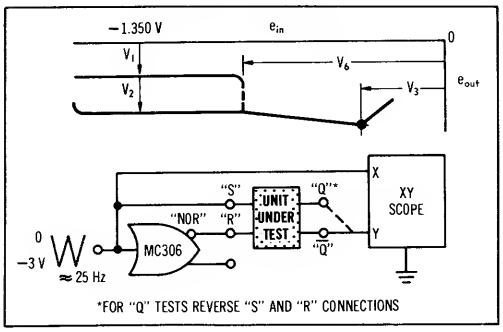


MC314

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

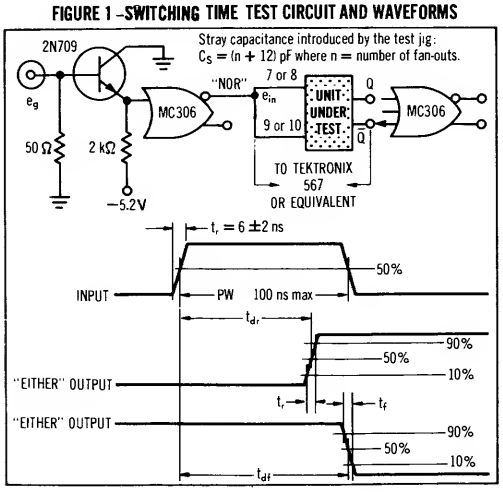


FIGURE 2 – INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

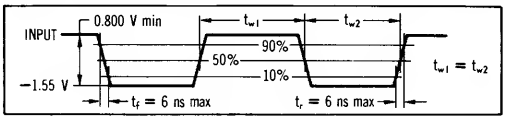


FIGURE 3 – SENSITIVITY (NO TOGGLE)

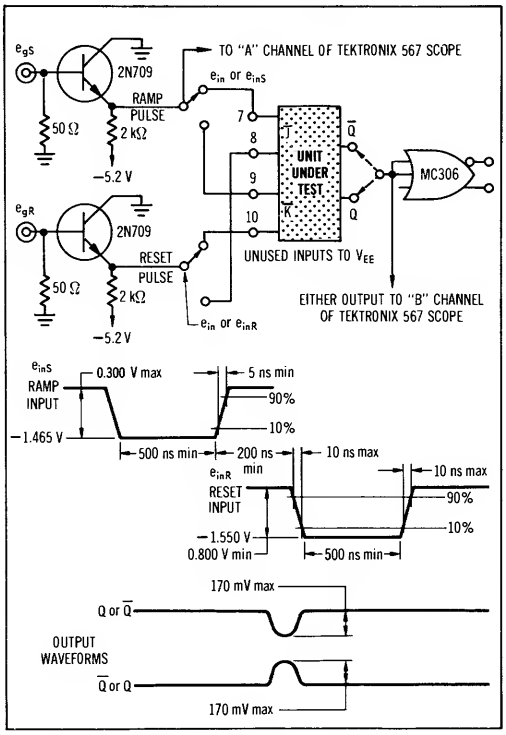
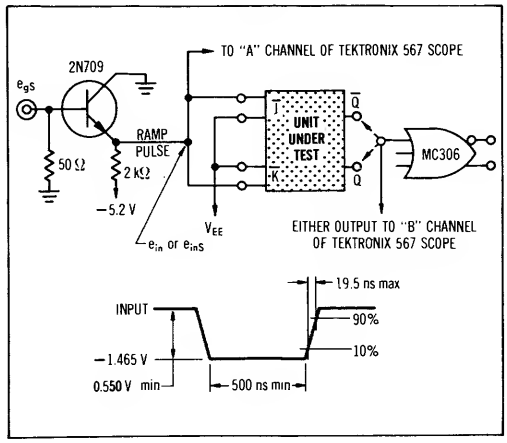


FIGURE 4 – SENSITIVITY (TOGGLE)



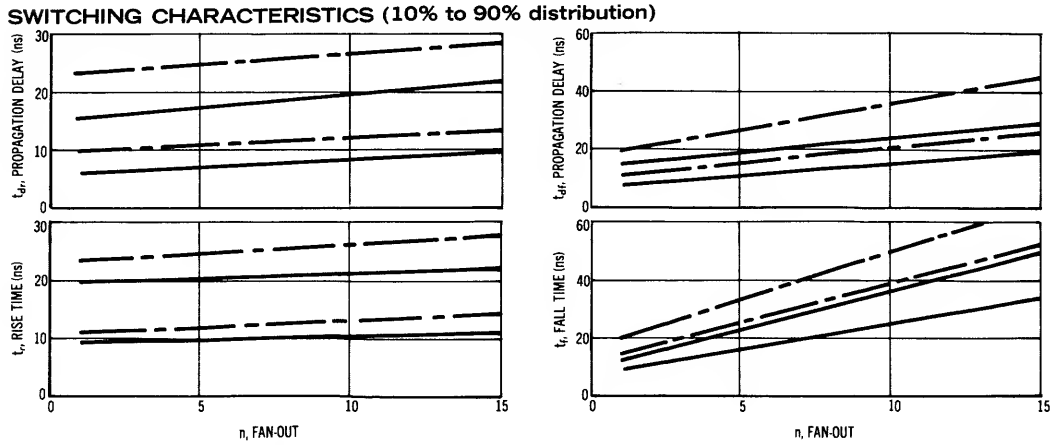
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
−55°C	—	−0.945	−1.450	−5.20
+25°C	−0.690	−0.795	−1.350	−5.20
+125°C	—	−0.655	−1.300	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	28.5	—	28.5	—	27.5	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"Q" Logical "0" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	1③	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6③	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5④	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.060	Volts
"$\bar{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4④	3	$\triangle V_1$ (4)	—	−0.055	—	−0.055	—	−0.060	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.50	—	−0.65	—	−0.75	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.50	—	−0.65	—	−0.75	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	−1.16	−1.34	−1.09	−1.21	−0.93	−1.07	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5	—	1,2,6,9	—	—	3	f_{Tog}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5	—	1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{dr} (4,5)	11.0	16.0	12.0	16.0	14.0	24.0	ns
	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{df} (4,5)	12.0	16.0	13.0	16.0	15.0	24.0	↓
Rise Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_r (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	
Fall Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	16.0	12.5	16.0	15.0	26.0	

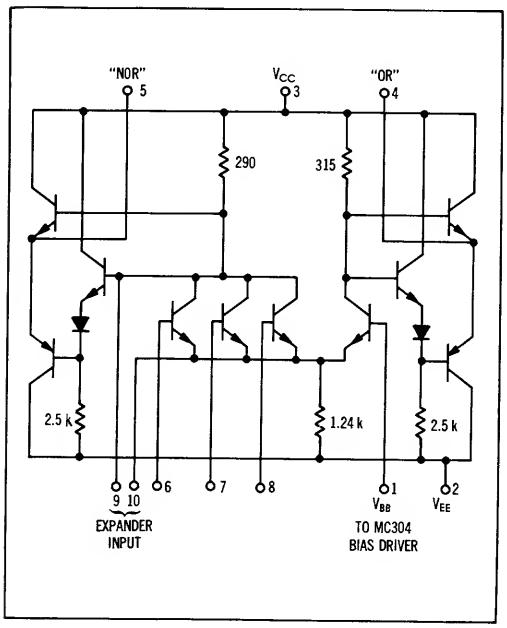
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
④ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ⑤ Input voltage is adjusted to obtain $dV_I / dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

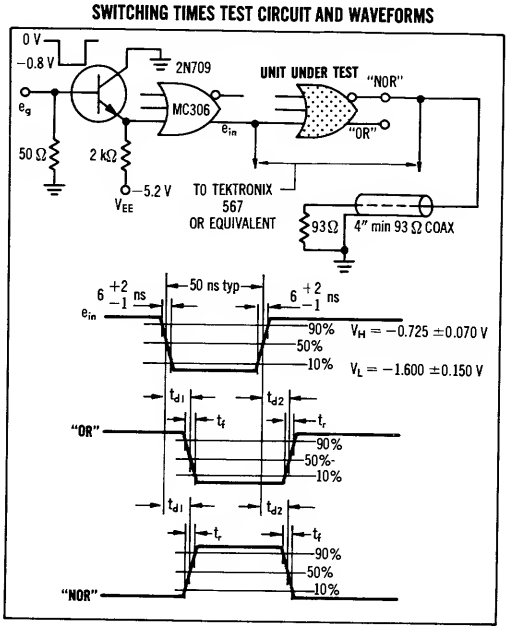


MC315

Line driver for driving lines of 93 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

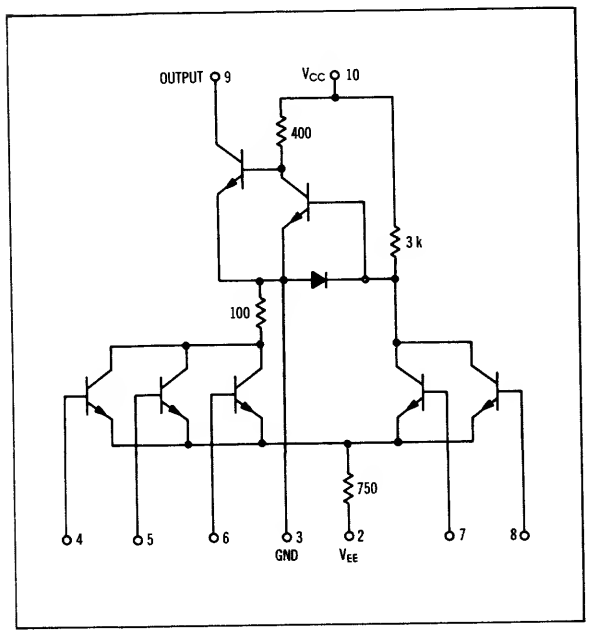
	Test Conditions Vdc ±1%				
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00

Characteristic	V_H Pin No	$V_{i\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L① Pin No	Ground Pin No	Symbol Pin No in ( )	−55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8	1	4,5	3	I_E (2)	—	45	—	45	—	45	mAdc
Input Current	6	—	—	2,7,8	1	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_1 (6)	−0.805	−0.945	−0.670	−0.795	−0.505	−0.655	Vdc
	—	—	7	2,6,8	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_4 (6)	−1.540	−1.850	−1.450	−1.750	−1.320	−1.675	Vdc
	—	7	—	2,6,8	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_4 (8)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_5 (6)	−0.805	−0.945	−0.670	−0.795	−0.505	−0.655	Vdc
	—	7	—	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_5 (8)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_2 (6)	−1.540	−1.850	−1.450	−1.750	−1.320	−1.675	Vdc
	—	—	7	2,6,8	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_2 (8)							
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	10.0	20.0	10.0	20.0	15.0	30.0	ns
	6	4	—	2,7,8	1	—	3	t_{d1} (4)	12.0	25.0	12.0	25.0	17.0	34.0	↓
	6	5	—	2,7,8	1	—	3	t_{d2} (5)	12.0	25.0	12.0	25.0	13.0	30.0	
	6	4	—	2,7,8	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	25.0	
Rise Time	6	5	—	2,7,8	1	—	3	t_r (5)	13.0	25.0	13.0	25.0	16.0	31.0	
	6	4	—	2,7,8	1	—	3	t_r (4)	10.0	20.0	10.0	20.0	14.5	26.0	
Fall Time	6	5	—	2,7,8	1	—	3	t_f (5)	15.0	35.0	15.0	35.0	20.0	40.0	
	6	4	—	2,7,8	1	—	3	t_f (4)	15.0	35.0	15.0	35.0	20.0	40.0	

Pins not listed are left open. ①Output is loaded with a 93-ohm resistor.

MC316

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6V lamps.



ELECTRICAL CHARACTERISTICS

		Test Conditions						
		Vdc ±1%						mAdc
@ Test Temperature	−55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	100
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100
	+125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	50

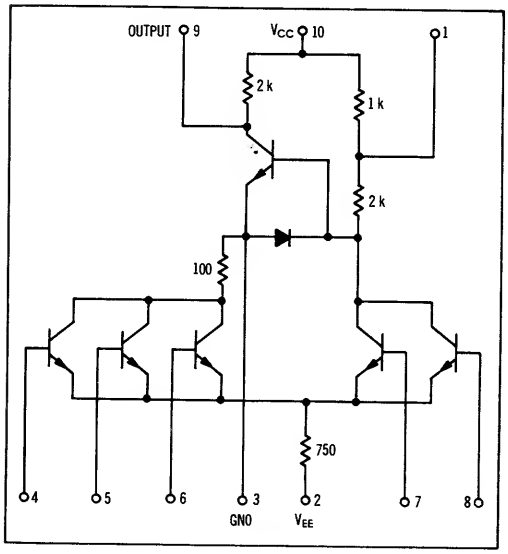
Characteristic	V_H Pin No	$V_{f\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L ② Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	21.0	—	21.0	—	20.5	
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.0	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, Luw	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	0.8	
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	10,9①	—	3	V_{OH} (5)	—	—	—	↓	—		↓
	—	6	—	2,4,5,7	8	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—		↓
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—		↓

Pins not listed are left open. ①Pin 9 is connected to V_{CC} through a 10 k-ohm resistor.

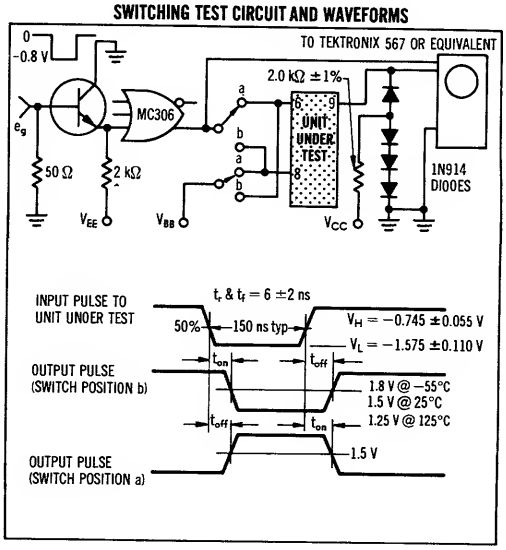
②I_L specified for ambient temperature conditions. I_L = 100 mAdc at T_C = +125°C is acceptable, requiring a heat sink.

MC317

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS



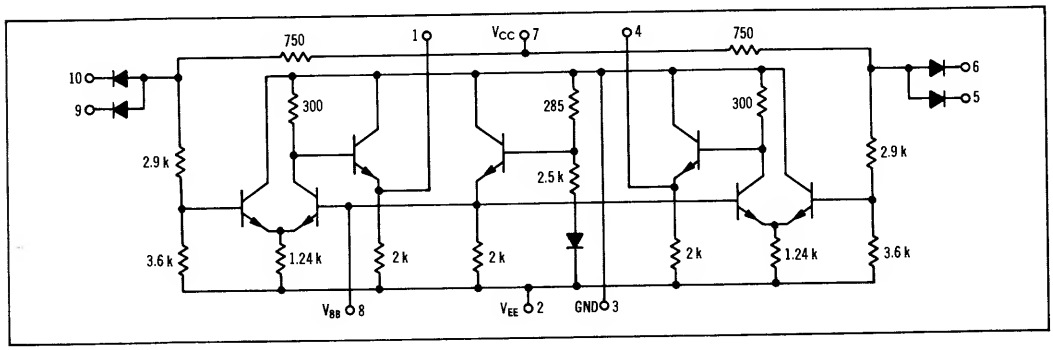
ELECTRICAL CHARACTERISTICS

	Test Conditions						
	Vdc ±1%						mAdc
@ Test Temperature −55°C	—	−0.945	−1.450	−5.20	−1.25	+6.0	10
@ Test Temperature +25°C	−0.690	−0.795	−1.350	−5.20	−1.15	+6.0	10
@ Test Temperature +125°C	—	−0.655	−1.300	−5.20	−1.00	+6.0	10

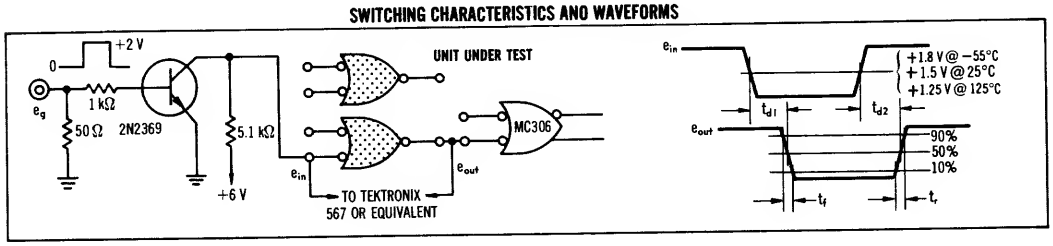
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_m Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.0	—	7.0	—	6.8	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.0	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,8	6	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,6,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,8	7	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	8	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on}	27.5	40.0	27.5	35.0	29.5	35.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓
	8	9	—	2,4,5,7	6	10	—	3	t_{off}	25.0	40.0	26.0	35.0	27.0	40.0	↓

MC318

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%			
@ Test Temperature −55°C	+0.45	+5.0	−5.20	+6.0
@ Test Temperature +25°C	+0.45	+5.0	−5.20	+6.0
@ Test Temperature +125°C	+0.45	+5.0	−5.20	+6.0

Characteristic	V Pin No	V Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits −55°C Min	−55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	—	—	2	7	3	I_C (7)	—	4.0	—	4.0	—	3.9	mAdc
	—	—	2	7	3	I_E (2)	—	24.0	—	24.0	—	23.3	mAdc
Input Load Current	—	—	2	7	3,5	I_L (5)	—	—	—	8.0	—	—	mAdc
	—	—	2	7	3,6	I_L (6)	—	—	—	↓	—	—	↓
	—	—	2	7	3,9	I_L (9)	—	—	—		—	—	
	—	—	2	7	3,10	I_L (10)	—	—	—		—	—	
Input Reverse Current	—	—	2	5,7	3,6	I_R (5)	—	—	—	0.5	—	2.0	μAdc
	—	—	2	6,7	3,5	I_R (6)	—	—	—	↓	—	↓	↓
	—	—	2	7,9	3,10	I_R (9)	—	—	—		—		
	—	—	2	7,10	3,9	I_R (10)	—	—	—		—		
"OR" Logical "1" Output Voltage	—	5	2	7	3	V_S (4)	−0.825	−0.945	−0.690	−0.795	−0.525	−0.655	Vdc
	—	6	2	7	3	V_S (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	2	7	3	V_S (1)							
	—	10	2	7	3	V_S (1)							
"OR" Logical "0" Output Voltage	5	—	2	7	3	V_2 (4)	−1.560	−1.850	−1.465	−1.750	−1.340	−1.675	Vdc
	6	—	2	7	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	9	—	2	7	3	V_2 (1)							
	10	—	2	7	3	V_2 (1)							
Bias Voltage Output Current	—	—	2	7	3	V_{BB} (8)	−1.19	−1.32	−1.09	−1.22	−0.95	−1.08	Vdc
							↓	↓	↓	↓	↓	↓	↓
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5	4	2	7	3	t_{d1} (4)	16.5	27.0	15.0	23.0	19.0	28.0	ns
	9	1	2	7	3	t_{d1} (1)	16.5	27.0	15.0	23.0	19.0	28.0	↓
	5	4	2	7	3	t_{d2} (4)	13.0	20.0	15.5	23.0	20.0	31.0	
	9	1	2	7	3	t_{d2} (1)	13.0	20.0	15.5	23.0	20.0	31.0	
Rise Time	5	4	2	7	3	t_r (4)	8.0	15.0	7.0	13.0	9.5	16.0	
	9	1	2	7	3	t_r (1)	8.0	15.0	7.0	13.0	9.5	16.0	
Fall Time	5	4	2	7	3	t_f (4)	8.0	14.0	7.5	13.0	10.0	17.0	
	9	1	2	7	3	t_f (1)	8.0	14.0	7.5	13.0	10.0	17.0	

Pins not listed are left open.

MECL

MC350 SERIES

INDEX

FUNCTIONS AND CHARACTERISTICS

V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C

Function	Type ①	DC Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg	Case
GATES					
5-Input OR/NOR Gate	MC351	25	7.5	37	602B,606
3-Input OR/NOR Gate	MC356	↓	7.5	37	↓
3-Input OR/NOR Gate	MC357		7.5	15	
Dual 2-Input NOR Gate	MC359		7.0	54	
Dual 2-Input NOR Gate	MC360		7.0	54	
Dual 2-Input NOR Gate	MC361		7.0	41	
Dual 3-Input NOR Gate (With Internal Bias)	MC362A		7.5	70	
Quad 2-Input NOR Gate	MC363F		7.0	125	607
Dual 4-Input High-Speed Gate	MC369F	100	3.0	250	607
Dual 2-Input High-Speed Gate	MC369G	100	3.0	250	602B
FLIP-FLOPS					
R-S Flip-Flop	MC352A	25	11	42	602B,606
AC-Coupled J-K Flip-Flop	MC358A	↓	8.5	87	↓
AC-Coupled J-K Flip-Flop	MC364		12	118	
HALF-ADDER					
Half-Adder	MC353	25	7.5	63	602B,606
GATE EXPANDER					
5-Input Gate Expander	MC355	—	4.5	—	602B,606
DRIVERS					
Bias Driver	MC354	25	—	18	602B,606
Line Driver	MC365	—	14	270 ②	↓
Lamp Driver	MC366	—	—	135	
Dual 4-Input Clock Driver	MC369F	100	3.0	250	607
Dual 2-Input Clock Driver	MC369G	100	3.0	250	602B
TRANSLATORS					
Level Translator — MECL to Saturated Logic	MC367	7 (DTL)	27.5	63	602B,606
Level Translator — Saturated Logic to MECL	MC368	25 (MECL)	17	105	602B,606

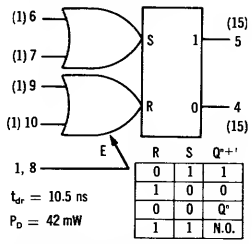
① G suffix denotes Metal Can, F suffix denotes Flat Package. (i.e., MC351G = Metal Can, MC351F = Flat Package.)
② With 50-ohm load (each side)

POSITIVE LOGIC: V_H is a logical "1", V_L is a logical "0"
NEGATIVE LOGIC: V_H is a logical "0", V_L is a logical "1"

The logic diagrams shown describe the circuits of the MC350 line and permit quick selection of those circuits required for the implementation of this particular logic system. Pertinent information such as logic equations, typical time delay, typical power dissipation, and truth tables is provided to show line compatibility. Package pin numbers and fan-in and fan-out for each device are specified on each logic diagram. The numbers at the ends of the terminals are package pin numbers. The numbers in parentheses indicate ac loading factors at each terminal.

MECL circuits require a bias voltage which, for best results, should be obtained from a regulated, temperature-compensated, bias supply. A bias driver, type MC354, is included in the MECL line to provide this function when the bias driver is not contained in the logic element. Specifications for the bias driver are included in this section of the Data Book.

MC352A — R-S FLIP-FLOP

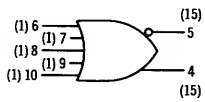


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.O.

t_{dr} = 10.5 ns
P_D = 42 mW

DC Set-Reset flip-flop with expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

MC351 — 5-INPUT GATE



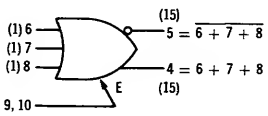
$5 = \overline{6 + 7 + 8 + 9 + 10}$

$4 = 6 + 7 + 8 + 9 + 10$

t_{dl} = 7.5 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC356 — 3-INPUT GATE



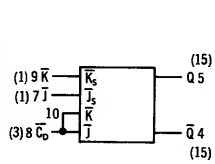
t_{dl} = 7.0 ns
P_D = 37 mW

Provides the positive logic "NOR" function and its complement simultaneously.

MC358A — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

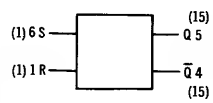
$\overline{J}_S$	$\overline{K}_S$	$\overline{C}_D$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}_S$ and $\overline{K}_S$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}_S$ and $\overline{K}_S$ inputs would be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

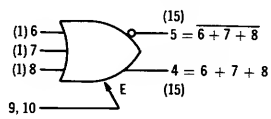
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.O.



t_{dr} = 7.5 ns
P_D = 87 mW

AC-Coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.

MC357 — 3-INPUT GATE



t_{dl} = 7.0 ns
P_D = 15 mW

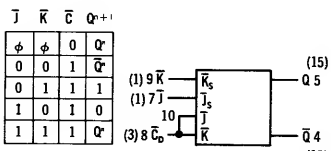
*No pull-down resistors

Provides the positive logic "NOR" function and its complement simultaneously. Same as MC356, with pull-down resistors omitted, permitting a reduction of power dissipation (see schematic diagram on the data sheet).

MC364 — AC-COUPLED J-K FLIP-FLOP

CLOCKED J-K OPERATION

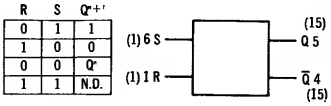
$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n



The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} − 0.6 volts)

R-S OPERATION

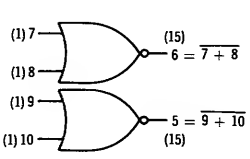
R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.



t_{dr} = 12 ns
P_D = 118 mW

High-speed ac-coupled J-K flip-flop with dc Set and Reset inputs for counter and shift register applications up to 30 MHz operation.

MC359 — DUAL 2-INPUT GATE

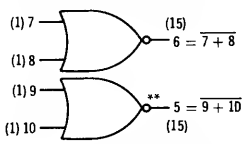


t_{dl} = 6.5 ns
P_D = 27 mW/gate

Provides the positive logic "NOR" function.

LOGIC DESCRIPTION (continued)

MC360 — DUAL 2-INPUT GATE

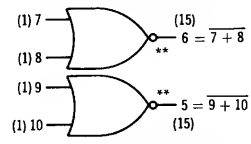


**Dptional pull-down resistor. If resistor is desired, connect pin 4 to pin 5.

t_{pl} = 6.5 ns P_D = 27 mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor optional (see schematic diagram on the data sheet).

MC361 — DUAL 2-INPUT GATE

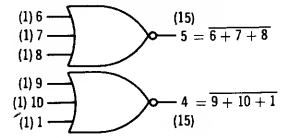


**Dptional pull-down resistor If resistor is desired, connect pin 4 to pin 5 or pin 6.

t_{pl} = 6.5 ns P_D = 21 mW/gate

Provides the positive logic "NOR" function. Same as MC359 with one output pull-down resistor omitted and the second optional (see schematic diagram on the data sheet).

MC362A — DUAL 3-INPUT GATE

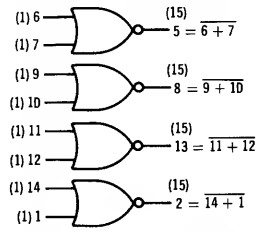


t_{pl} = 7.5 ns

P_D = 35 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver. This gate without the bias driver is available as the MC362.

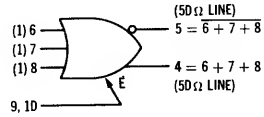
MC363F — QUAD 2-INPUT GATE



t_{pl} = 6.5 ns P_D = 31 mW/gate

Provides the positive logic "NOR" function, and features an internal bias driver.

MC365 — LINE DRIVER

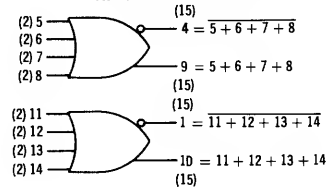


t_{pl} = 14 ns

P_D = 270 mW (with 50 Ω load)

Drives lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.

MC369F — HIGH-SPEED CLOCK DRIVER OR DUAL 4-INPUT GATE

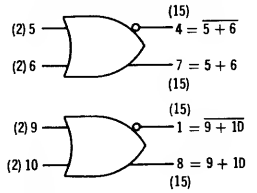


t_{pl} = 3 ns

P_D = 125 mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC369G — HIGH-SPEED CLOCK DRIVER OR DUAL 2-INPUT GATE

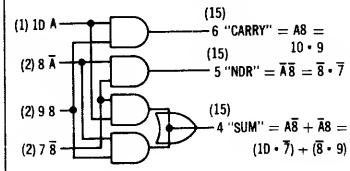


t_{pl} = 3ns

P_D = 125 mW/gate

Provides the positive logic "NOR" function and its complement simultaneously.

MC353 — HALF-ADDER

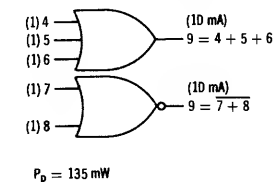


t_{pl} = 7 ns

P_D = 63 mW

Provides the "SUM", "CARRY", and "NDR" functions simultaneously. If complement inputs are not used, an undefined state can occur.

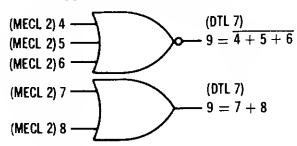
MC366 — LAMP DRIVER



P_D = 135 mW

Capable of driving 6-volt lamps. Positive "NDR" function is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs. Positive "DR" is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs.

MC367 — LEVEL TRANSLATOR

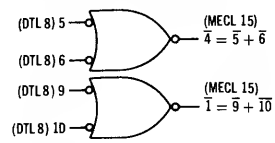


t_{dr} = 30 ns

P_D = 63 mW

Intended for converting non-saturated MECL signal levels to saturated logic levels. Positive "NDR" function is obtained by applying V_{BB} to pin 7 or 8, with pins 4, 5, and 6 used as inputs. Positive "DR" is obtained by applying V_{BB} to pin 4, 5, or 6, with pins 7 and 8 used as inputs.

MC368 — LEVEL TRANSLATOR

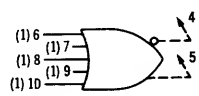


t_{pl} = 17 ns

P_D = 105 mW

Intended for converting saturated logic levels to non-saturated MECL signal levels. By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at −1.55 V and logical "1" at −0.75 V.

MC355 — 5-INPUT EXPANDER



t_{pl} = 5 ns

For use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five. For highest performance, a maximum of three expander units per gate is recommended.

CIRCUIT DESCRIPTION

The MECL line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical MECL circuit comprises a differential-amplifier input, with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.

POWER-SUPPLY CONNECTIONS

Any one of the power supply nodes, V_{BB}, V_{CC}, or V_{EE} may be used as ground; however, the manufacturer has found it most convenient to ground the V_{CC} node. In such a case: $V_{CC} = 0$, $V_{BB} = -1.15$ V, $V_{EE} = -5.2$ V, as shown in the schematic diagram above.

SYSTEM LOGIC SPECIFICATIONS

The output logic swing of 0.8 V then varies from a low state of $V_L = -1.55$ V to a high state of $V_H = -0.75$ V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's". Then

"0" = −1.55 V
"1" = −0.75 V
} typical

Dynamic logic refers to a change of logic states. Dynamic "0" is a negative going voltage excursion and a dynamic "1" is a positive going voltage excursion.

CIRCUIT OPERATION

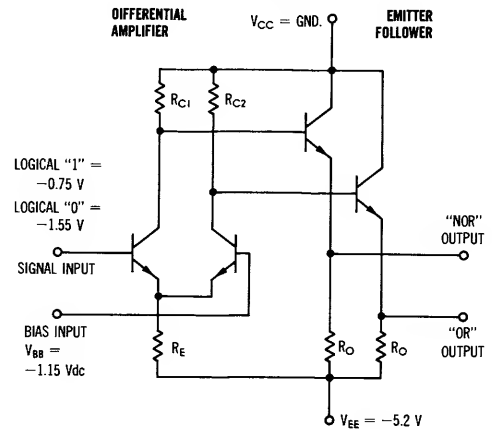
A fixed bias of −1.15 volts is applied to the "bias input" of the differential amplifier and the logic signals are applied to the "signal input". If a logical "0" is applied, the current through R_E is supplied by the fixed-biased transistor. A drop of 800 mV occurs across R_{C2}. The OR output then is −1.55 V, or one V_{BE} drop below 800 mV. Since no current flows in the "signal input" transistor, the NOR output is a V_{BE} drop below ground, or −0.75 volts. When a logical "1" level is applied to the "signal input", the current through R_{C2} is switched to the "signal input" transistor and a drop of 800 mV occurs across R_{C1}. The OR output then goes to −0.75 volts and the NOR output goes to −1.55 volts.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from a regulated, temperature-compensated bias driver, type MC354. The temperature characteristics of the bias driver compensate for any variations in circuit operating point over the temperature range or supply voltage changes, to insure that the threshold point is always in the center of the transition region. The bias driver can be used to drive up to 25 logic elements and should be employed for all elements except those with built-in bias networks.

BASIC MECL GATE CIRCUIT



FOR LOGICAL "1" INPUT, "NOR" OUTPUT = −1.55 V
"OR" OUTPUT = −0.75 V
FOR LOGICAL "0" INPUT, "NOR" OUTPUT = −0.75 V
"OR" OUTPUT = −1.55 V

DEFINITIONS

e_{in} AC signal applied to the input

e_{out} AC signal at the output

I_C Amount of current drawn from the positive power supply by the test unit

I_{CEX} Total collector leakage current exhibited by the gate expander when all inputs are at the negative supply potential

I_E Amount of current drawn from the test unit by the negative power supply

I_{in} Current drawn by the input of the test unit when a logical "1" (V_H) is applied to the input

I_L Current drawn from a node when that node is at ground potential

t_{d1} Time required for the output pulse to reach the 50% point of its leading edge when referenced to the 50% point of the input pulse leading edge

t_{d2} Time required for the output pulse to reach the 50% point of its trailing edge when referenced to the 50% point of the input pulse trailing edge

t_{df} Time required for a flip-flop output to reach the 50% point of its negative going edge when referenced to the 50% point of the input pulse leading edge

t_{dr} Time required for a flip-flop output to reach the 50% point of its positive going edge when referenced to the 50% point of the input pulse leading edge

t_f Time required for the output pulse to go more negative from its 90% point to its 10% point

t_r Time required for the output pulse to go more positive from its 10% point to its 90% point

V_1 "NOR" output voltage – logical "1" level output voltage when a logical "0" level (V_L) is applied to the input

V_2 "OR" output voltage – logical "0" level output voltage when a logical "0" level (V_L) is applied to the input

V_3 Saturation breakpoint voltage which corresponds to the "NOR" output characteristic where the rate of change in the output voltage to the rate of change in input voltage is zero

V_4 "NOR" output voltage – logical "0" level output voltage when a logical "1" level ($V_{1\ max}$) level is applied to the input

V_5 "OR" output voltage – logical "1" level output voltage when a logical "1" ($V_{1\ max}$) level is applied to the input

V_6 Output latch voltage – input voltage to a flip-flop which causes the output voltage to change from a logical "1" level to a logical "0" level and corresponds to the point where the rate of change in the output voltage to the rate of the input voltage approaches infinity

V_H Logical "1" input voltage

V_L Logical "0" input voltage

V_{OH} High-level output voltage when the saturated logic circuit output is in an "off" condition

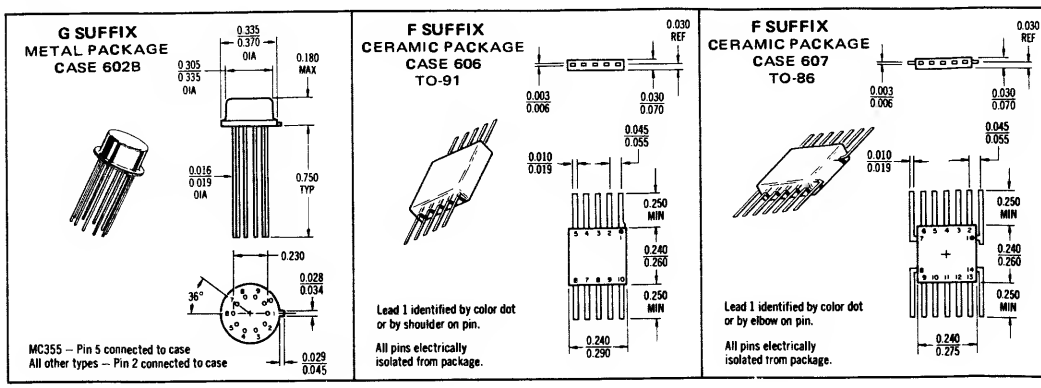
V_{OL} Low-level output voltage when the saturated logic output circuit is in an "on" condition

ΔV_1 Change in the "1" level output voltage as the
ΔV_5 load is varied from no load to full load

PACKAGES

All MECL integrated circuits are available in both the TO-91, 10-lead flat package and the 10-lead metal package. To order the flat package, add suffix "F" to basic type number; to order metal package, add suffix "G".

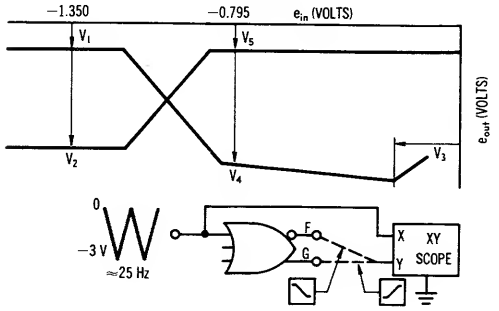
Exceptions: Types MC363F and MC369F are available only in the TO-86, 14-lead flat package; type MC369G is available only in the metal package.

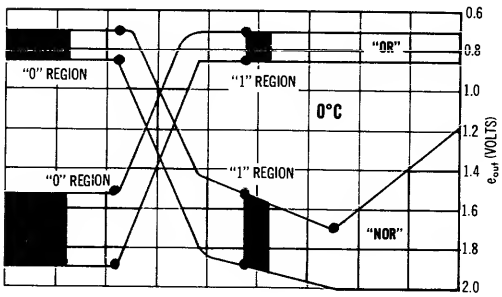


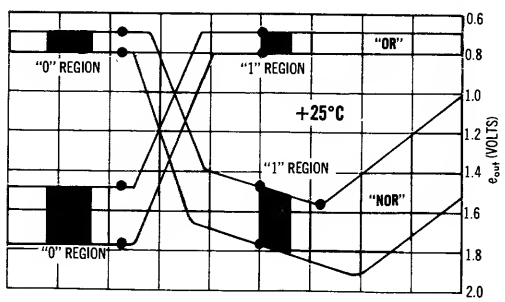
WORST-CASE TRANSFER CHARACTERISTICS

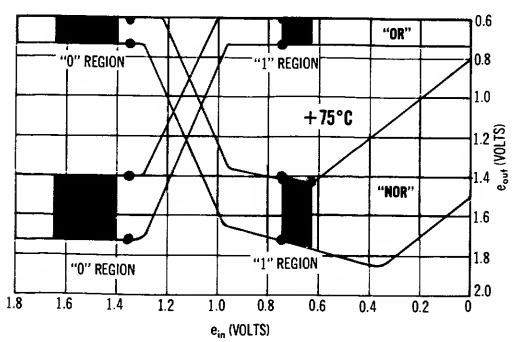
The following graphs show minimum and maximum limits of major parameters associated with the transfer characteristics of the MECL line. Min-Max limits, given at three different temperatures can be interpreted for design purposes as 10% to 90% spreads at all points on the curve except for guaranteed points in the Electrical Characteristics tables.

DEFINITIONS









MAXIMUM RATINGS

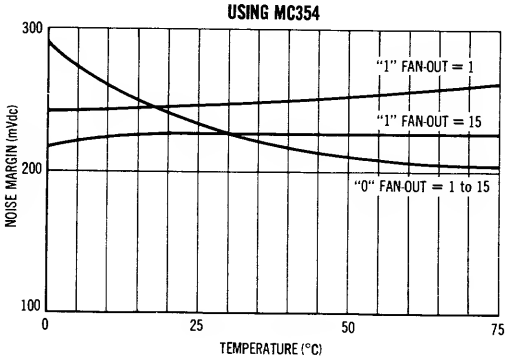
Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−10	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 Vdc to V_{EE}	Vdc
Output Source Current	I_O	20	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
AC Fan-In (Expandable Gates)	m	18	—
AC Fan-Out* (Gates and Flip-Flops)	n	15	—

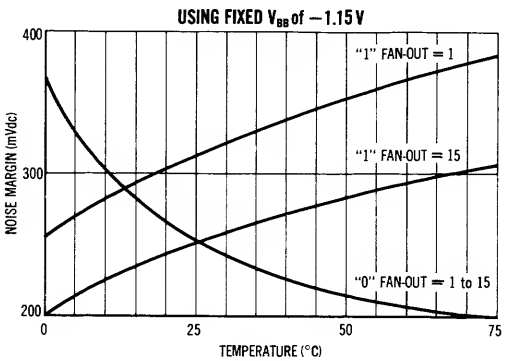
*Although a minimum dc fan-out of 25 is guaranteed in each electrical specification, it is recommended that the maximum ac fan-out of 15 be used for high-speed operation.

NOISE MARGINS (90 PERCENTILE)

The following graphs show worst-case Noise Margins as a function of temperature and fan-out. Top graph illustrates the advantage gained through use of MC354 bias driver, as compared with non-compensated fixed bias source, bottom.

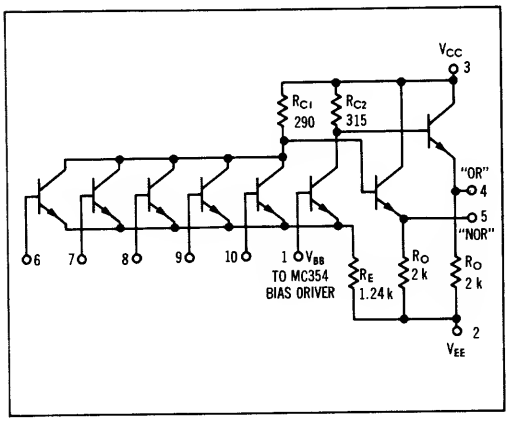
Note: Any unused input should be connected to V_{EE}.



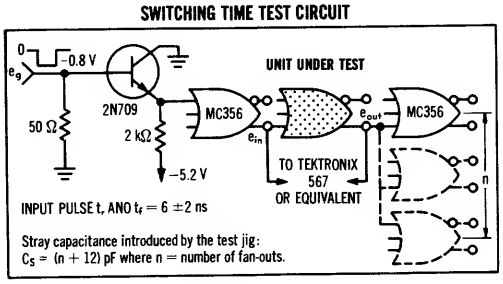


MC351

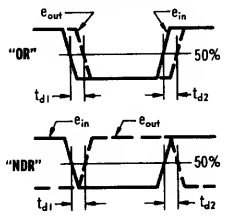
A 5-input gate that provides the positive logic "OR" function and its complement simultaneously.



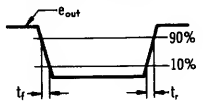
SWITCHING TIME TEST CIRCUIT



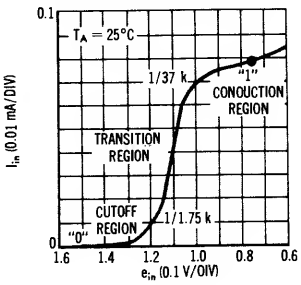
PROPAGATION DELAY



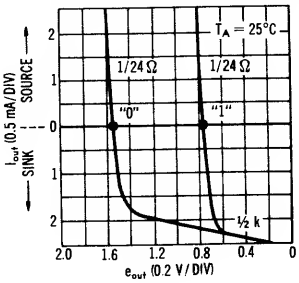
RISE AND FALL TIME



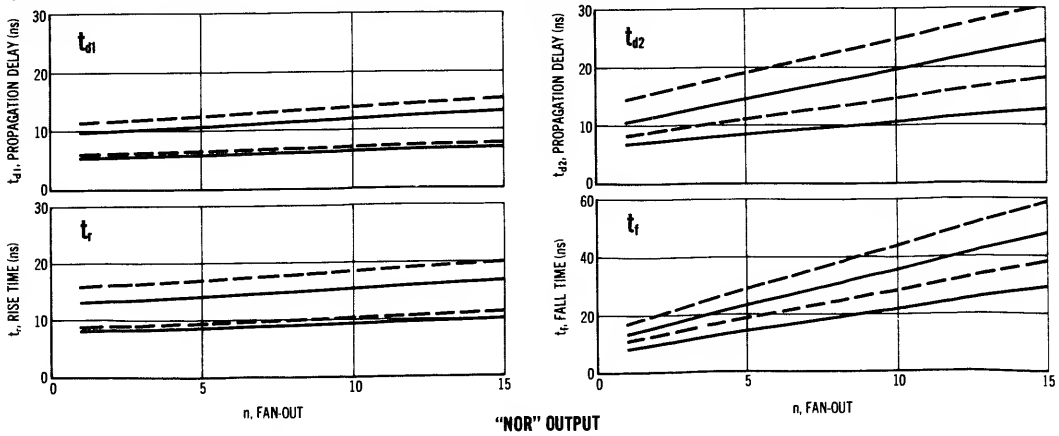
TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"NOR" OUTPUT

0°C and +25°C

+75°C

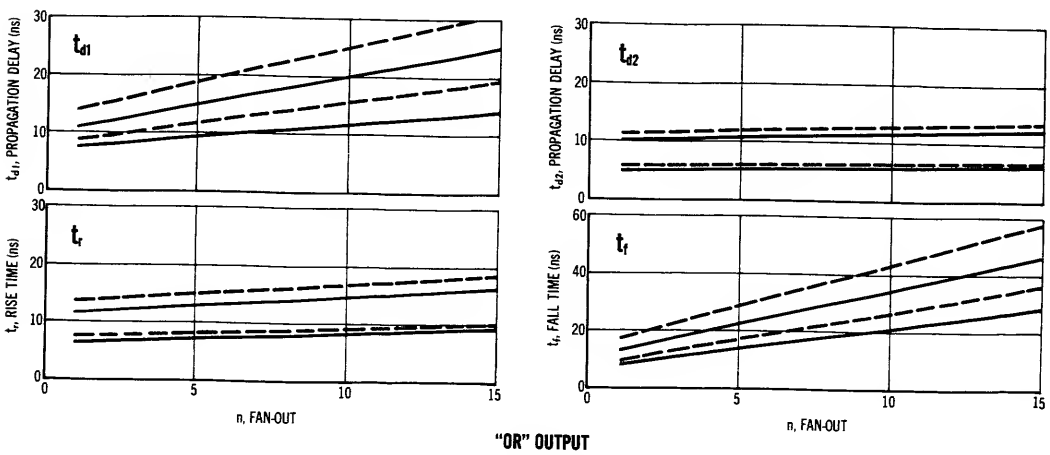
ELECTRICAL CHARACTERISTICS

@ Test Temperature	V_H Pin No	$V_{t\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Test Conditions Vdc ±1%																
0°C	—	−0.850	−1.350	−5.20	−1.18											
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15											
+75°C	—	−0.725	−1.350	−5.20	−1.08											
Power Supply Drain Current	—	—	—	2,6,7,8,9,10	1	—	—	3	I_E (2)	—	9.25	—	8.85	—	8.15	mAdc
Input Current	6	—	—	2,7,8,9,10	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7,9,10	1	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	2,6,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_1 (5)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_1 (5)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_4 (5)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_4 (5)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8,9,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,8,9,10	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7,9,10	1	—	—	3	V_5 (4)							
	—	9	—	2,6,7,8,10	1	—	—	3	V_5 (4)							
	—	10	—	2,6,7,8,9	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8,9,10	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8,9,10	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7,9,10	1	—	—	3	V_2 (4)							
	—	—	9	2,6,7,8,10	1	—	—	3	V_2 (4)							
	—	—	10	2,6,7,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	6	2,7,8,9,10	1	—	5③	3	$\triangle V_1$ (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8,9,10	1	—	4③	3	$\triangle V_5$ (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9,10	1	6①	—	3	V_3 (5)	—	− 0.51	—	− 0.55	—	− 0.63	Vdc
	—	—	—	2,6,8,9,10	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7,9,10	1	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,10	1	9①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9	1	10①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	4	—	2,7,8,9,10	1	—	—	3	t_{d1} (4)	9.0	12.5	9.0	12.5	9.5	16.0	ns
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d1} (5)	7.0	11.0	7.0	11.0	7.5	13.0	↓
	6	4	—	2,7,8,9,10	1	—	—	3	t_{d2} (4)	6.5	11.0	6.5	11.0	7.5	13.0	
	6	5	—	2,7,8,9,10	1	—	—	3	t_{d2} (5)	8.5	12.5	8.5	12.5	10.0	16.0	
Rise Time	6	4	—	2,7,8,9,10	1	—	—	3	t_r (4)	8.0	12.0	8.0	12.0	9.5	15.5	
	6	5	—	2,7,8,9,10	1	—	—	3	t_r (5)	9.5	14.5	10.0	14.5	11.0	17.0	
Fall Time	6	4	—	2,7,8,9,10	1	—	—	3	t_f (4)	9.5	15.0	10.0	15.0	11.0	17.5	
	6	5	—	2,7,8,9,10	1	—	—	3	t_f (5)	9.0	15.0	9.5	15.0	10.5	17.5	

Pins not listed are left open

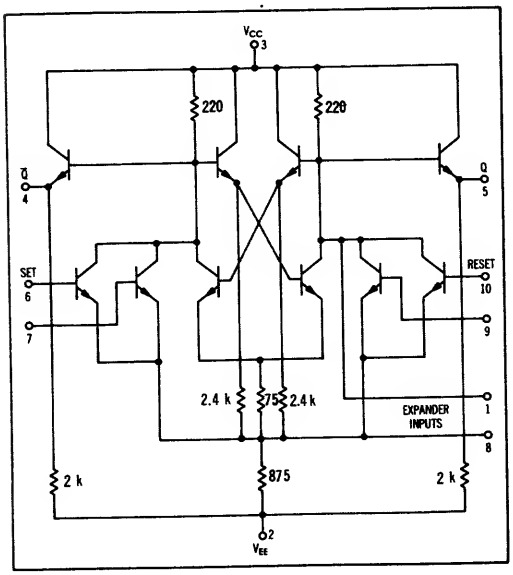
① Input voltage is adjusted to obtain dV "NOR / dV_{in} = "0".

③ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

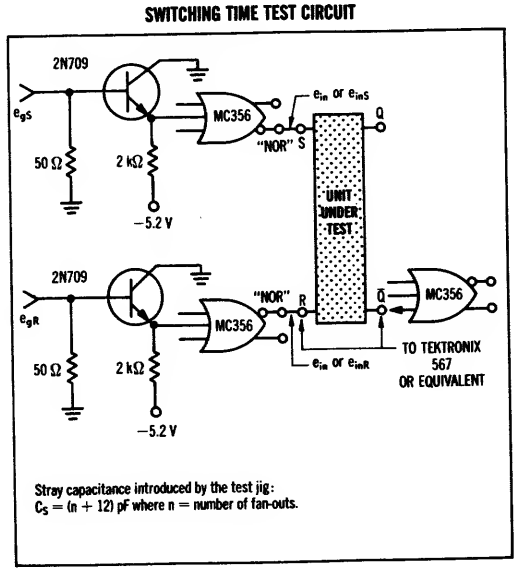


MC352A

DC Set-Reset flip-flop with an expandable input and buffered outputs. This flip-flop is available without buffered outputs as MC352.

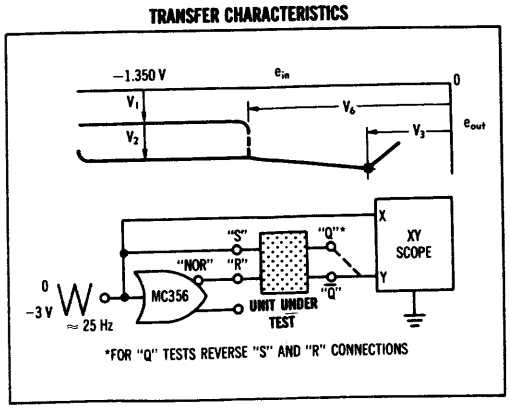


SWITCHING TIME TEST CIRCUIT



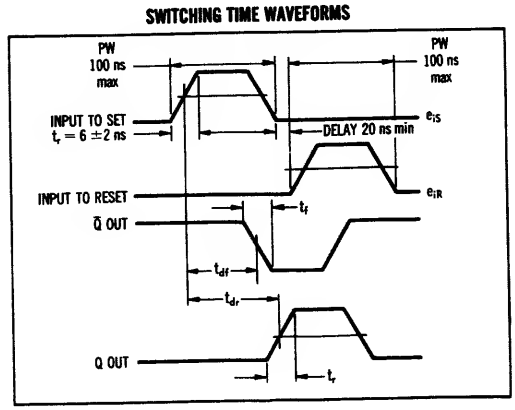
Stray capacitance introduced by the test jig:
$C_S = (n + 12)$ pF where n = number of fan-outs.

TRANSFER CHARACTERISTICS



*FOR "Q" TESTS REVERSE "S" AND "R" CONNECTIONS

SWITCHING TIME WAVEFORMS



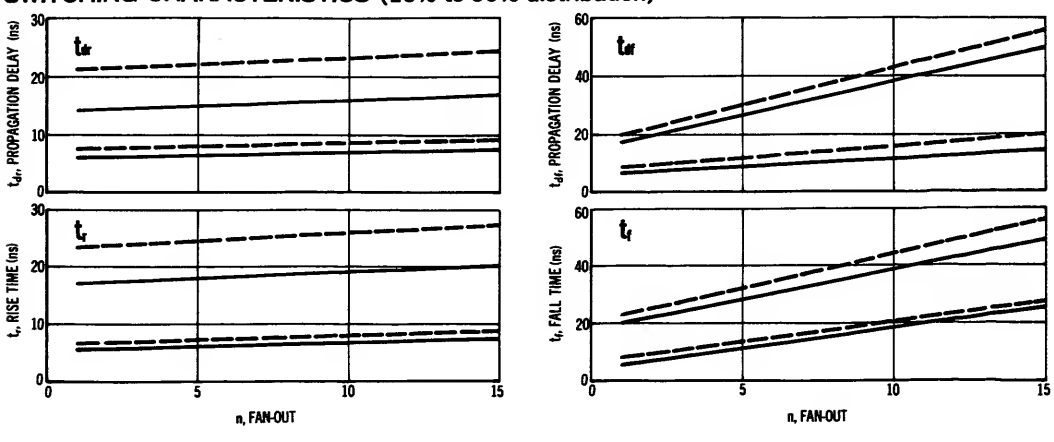
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L ⑤ Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,9,10	—	—	3	I_R (6)	—	10.35	—	10.35	—	9.52	mAdc
Input Current	6	—	—	2,7,9,10	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,9,10	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	9	—	—	2,6,7,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,6,7,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	10	2,6,7,9	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\overline{Q}$" Logical "1" Output Voltage	—	—	9	2,6,7,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,6,7,9	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\overline{Q}$" Logical "0" Output Voltage	—	—	6	2,7,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	2,7,9,10	—	5③	3	ΔV_1 (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\overline{Q}$" Output Voltage Change	—	10	—	2,6,7,9	—	4③	3	ΔV_1 (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (5)	—	−0.61	—	−0.65	—	−0.73	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,7,9	6,10①	—	3	V_3 (4)	—	−0.61	—	−0.65	—	−0.73	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,9	6,10④	—	3	V_4 (6,10)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6,10	4,5	—	2,7,9	—	—	3	t_{dr} (4,5)	10.0	16.0	10.5	16.0	13.5	22.0	ns
	6,10	4,5	—	2,7,9	—	—	3	t_{df} (4,5)	11.0	19.5	11.5	19.5	14.0	22.0	↓
Rise Time	6,10	4,5	—	2,7,9	—	—	3	t_r (4,5)	11.0	19.0	11.5	19.0	13.5	26.0	
Fall Time	6,10	4,5	—	2,7,9	—	—	3	t_f (4,5)	12.0	19.5	12.5	19.5	14.0	26.0	

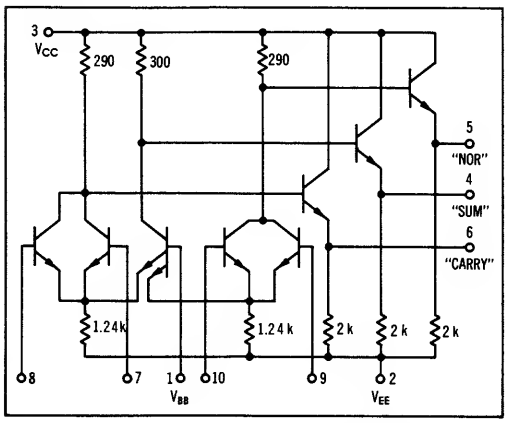
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "Q" / dV_{in} = 0; dV "$\overline{Q}$" / dV_{in} = 0. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{I\,max}$ to set output, then V_L for measurement. ④ Input voltage is adjusted to obtain dV_I / dV_{in} = ∞.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

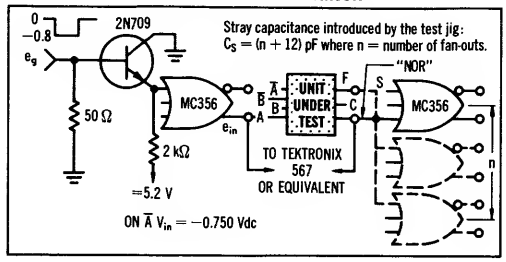


MC353

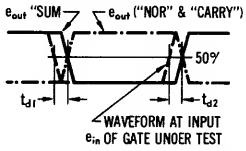
Half-adder that provides the "SUM", "CARRY", and "NOR" functions simultaneously.



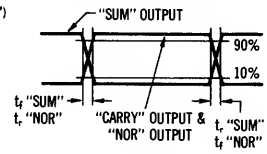
SWITCHING TIMES TEST CIRCUIT



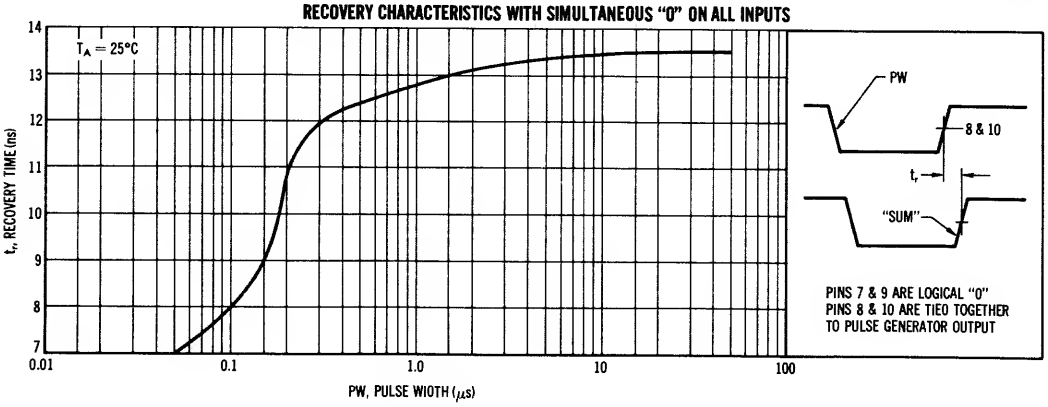
PROPAGATION DELAY



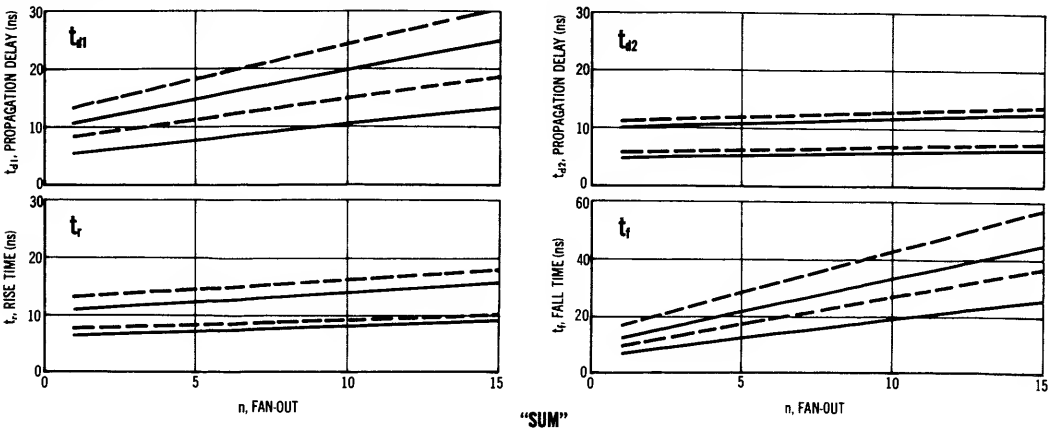
RISE AND FALL TIMES



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS



SWITCHING CHARACTERISTICS (10% to 90% distribution)



"SUM"

0°C and +25°C

+75°C

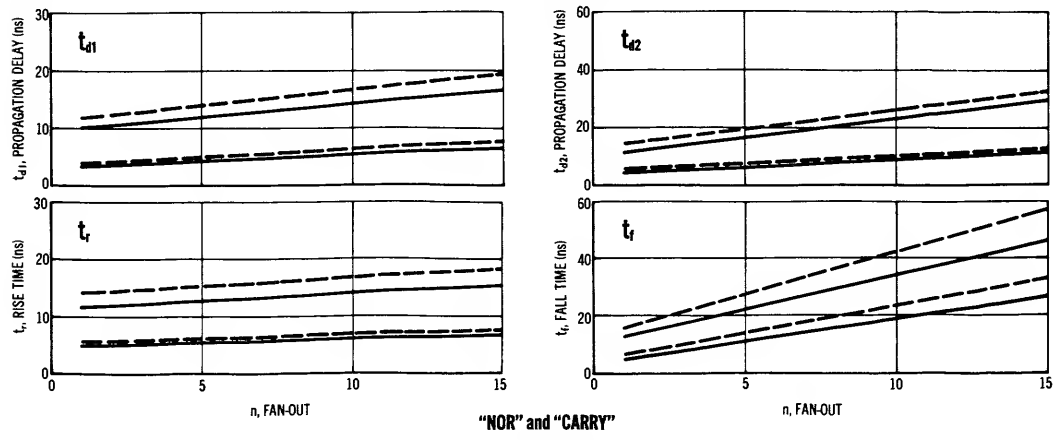
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%				
0°C	—	−0.850	−1.350	−5.20	−1.18
+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{f\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	15.9	—	15.3	—	14.1	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"NOR" Logical "0" Output Voltage	—	9	—	2,7,8,10	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	10	—	2,7,8,9	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"CARRY" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"CARRY" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_4 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"SUM" Logical "1" Output Voltage	—	7,9	—	2,8,10	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	8,10	—	2,7,9	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"SUM" Logical "0" Output Voltage	—	7	10	2,8,9	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	10	2,7,9	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	8	2,7,10	1	—	—	3	V_2 (4)							
	—	10	7	2,8,9	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	10	—	2,7,8,9	1	—	5②	3	ΔV_1 (5)	—	0.055	—	0.055	—	0.065	Volts
"CARRY" Output Voltage Change (No load to full load)	—	—	7	2,8,9,10	1	—	6②	3	ΔV_1 (6)	—	0.055	—	0.055	—	0.065	Volts
"SUM" Output Voltage Change (No load to full load)	—	7,10	—	2,8,9	1	—	4②	3	ΔV_5 (4)	—	0.055	—	0.055	—	0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	0.510	—	0.550	—	0.630	Vdc
"CARRY" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	0.510	—	0.550	—	0.630	Vdc
Switching Times						Pulse In	Pulse Out			Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	—	—	—	2,7,8,9	1	10	5	3	t_{d1} (5)	6.5	11.0	6.5	11.0	7.0	13.0	ns
	—	—	—	2,8,9,10	1	7	6	3	t_{d1} (6)	6.5	11.0	6.5	11.0	7.0	13.0	↓
	—	7	—	2,8,9	1	10	4	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
	—	—	—	2,7,8,9	1	10	5	3	t_{d2} (5)	8.5	13.5	8.5	13.5	10.0	16.0	
	—	—	—	2,8,9,10	1	7	6	3	t_{d2} (6)	8.5	13.5	8.5	13.5	10.0	16.0	
	—	7	—	2,8,9	1	10	4	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	
Rise Time	—	—	—	2,7,8,9	1	10	5	3	t_r (5)	9.0	12.5	9.0	12.5	11.0	15.5	
	—	—	—	2,8,9,10	1	7	6	3	t_r (6)	9.0	12.5	9.0	12.5	11.0	15.5	
	—	7	—	2,8,9	1	10	4	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	
Fall Time	—	—	—	2,7,8,9	1	10	5	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	
	—	—	—	2,8,9,10	1	7	6	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	
	—	7	—	2,8,9	1	10	4	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	↓

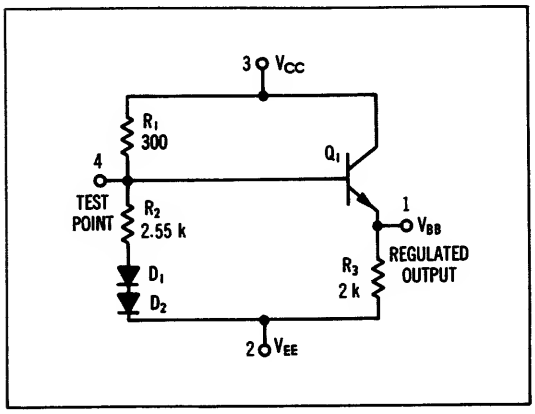
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{"NOR"}/dV_{in} = 0$ or $dV_{"CARRY"}/dV_{in} = 0$.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC354

Bias driver that compensates for changes in circuit parameters with temperature.



ELECTRICAL CHARACTERISTICS

		Test Conditions Vdc ±1%
@ Test Temperature	0°C	−5.20
	+25°C	−5.20
	+75°C	−5.20

Characteristic	V_{EE} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	2	—	3	I_E (2)	—	4.6	—	4.4	—	4.0	mAdc
Output Voltage	2	1①	3	V_{BB}	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc

Pins not listed are left open.

① Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

CIRCUIT DESCRIPTION

Circuit Operation:

The divider network R_1, R_2, D_1, D_2 compensates for temperature variations of the base-emitter voltages of Q_1, and of the driven gates, producing a bias voltage for the MECL logic circuits that maintains a constant set of dc operating conditions over the temperature range of 0 to +75°C. In addition, compensation for power supply variations is achieved, since the bias output voltage is derived from the system supply.

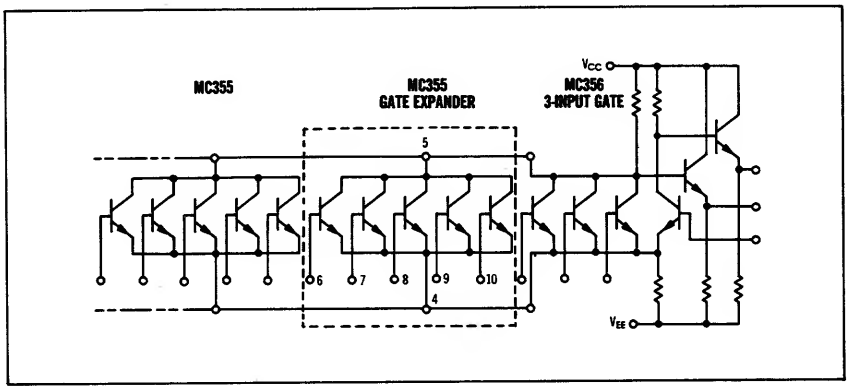
Either of the supply voltage nodes may be used as ground, however the ground potential of the bias driver must coincide with that of the logic system. Thus, if V_{CC} is grounded in the logic system, then —

$V_{CC} = 0$; $V_{EE} = -5.2$ V;

$V_{BB} = -1.15$ nominal output voltage at 25°C

MC355

A 5-input expander for use with the MC352A, MC356, MC357, and MC365. Each expander unit increases the fan-in of the basic gate by five.



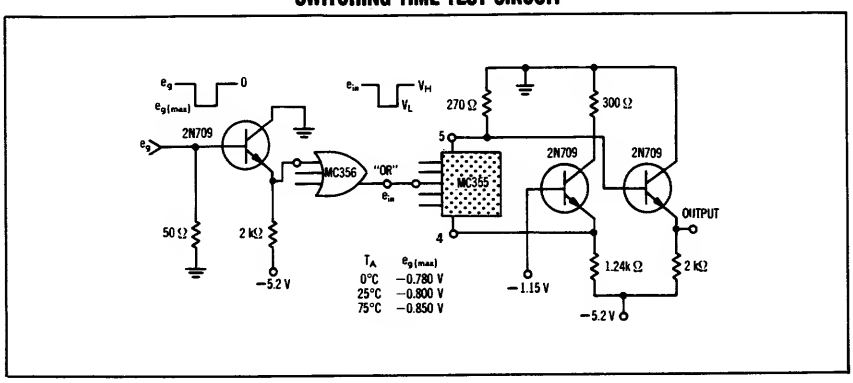
ELECTRICAL CHARACTERISTICS

	Test Conditions					
	Vdc ±1%					mAdc
@ Test Temperature 0°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +25°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33
@ Test Temperature +75°C	−2.0	−5.2	+2.0	+0.7	0.3	−1.33

Characteristic	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	V_{CS} Pin No	V_{BE} Pin No	I_E Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Base Leakage Current	4	6	—	—	—	—	5	I_{BL} (6)	—	0.5	—	0.5	—	2.0	μAdc
	4	7	—	—	—	—	5	I_{BL} (7)	—	↓	—	↓	—	↓	↓
	4	8	—	—	—	—	5	I_{BL} (8)	—		—		—		
	4	9	—	—	—	—	5	I_{BL} (9)	—		—		—		
	4	10	—	—	—	—	5	I_{BL} (10)	—		—		—		
Collector Leakage Current	—	—	5	—	6,7,8,9,10	—	4	I_{CEX} (5)	—	1.0	—	1.0	—	15.0	μAdc
Input Voltage	—	—	—	5	—	4	6	V_{BE} (4)	0.730	0.780	0.680	0.730	0.580	0.630	Vdc
	—	—	—	5	—	4	7	V_{BE} (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	—	5	—	4	8	V_{BE} (4)							
	—	—	—	5	—	4	9	V_{BE} (4)							
	—	—	—	5	—	4	10	V_{BE} (4)							
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	①	—	—	—	—	—	—	4.5	9.5	4.5	9.5	5.5	13.0	ns
	8	①	—	—	—	—	—	—	4.0	9.0	4.0	9.0	4.5	12.0	↓
Rise Time	8	①	—	—	—	—	—	—	8.5	13.0	8.5	13.0	9.0	15.0	
Fall Time	8	①	—	—	—	—	—	—	3.5	10.5	3.5	10.5	4.0	11.5	

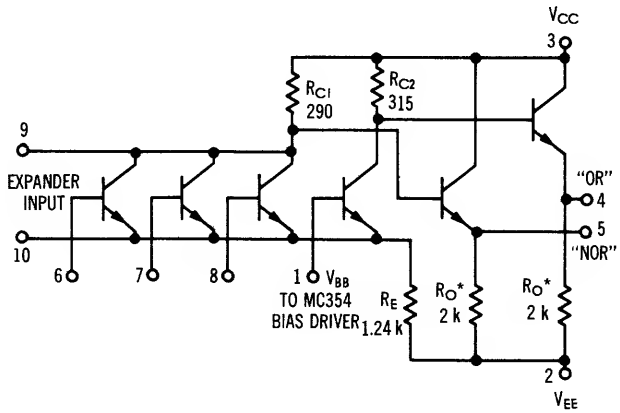
Pins not listed are left open. ①See Switching Time Test Circuit.

SWITCHING TIME TEST CIRCUIT



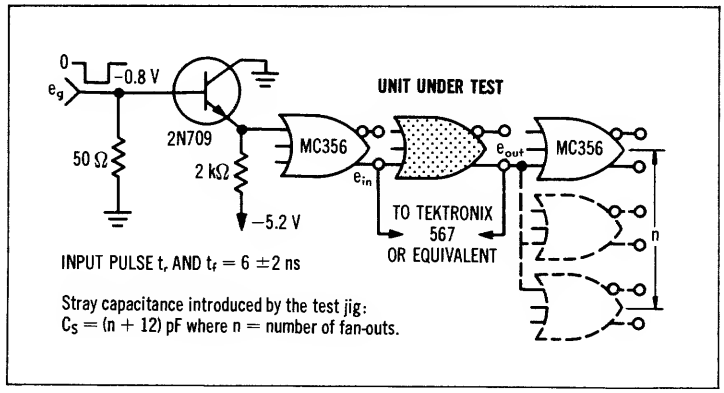
MC356 • MC357

Expandable 3-input gates that provide the positive logic "NOR" function and its complement simultaneously. MC357 omits output pull-down resistors, permitting reduction of power dissipation.

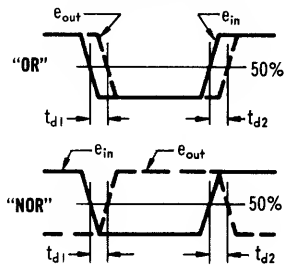


*Resistors R_O are omitted in MC357 circuits to permit reduction of Power Dissipation in systems where logic operations are performed at circuit outputs.

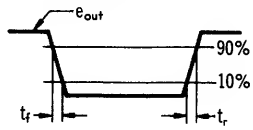
SWITCHING TIME TEST CIRCUIT



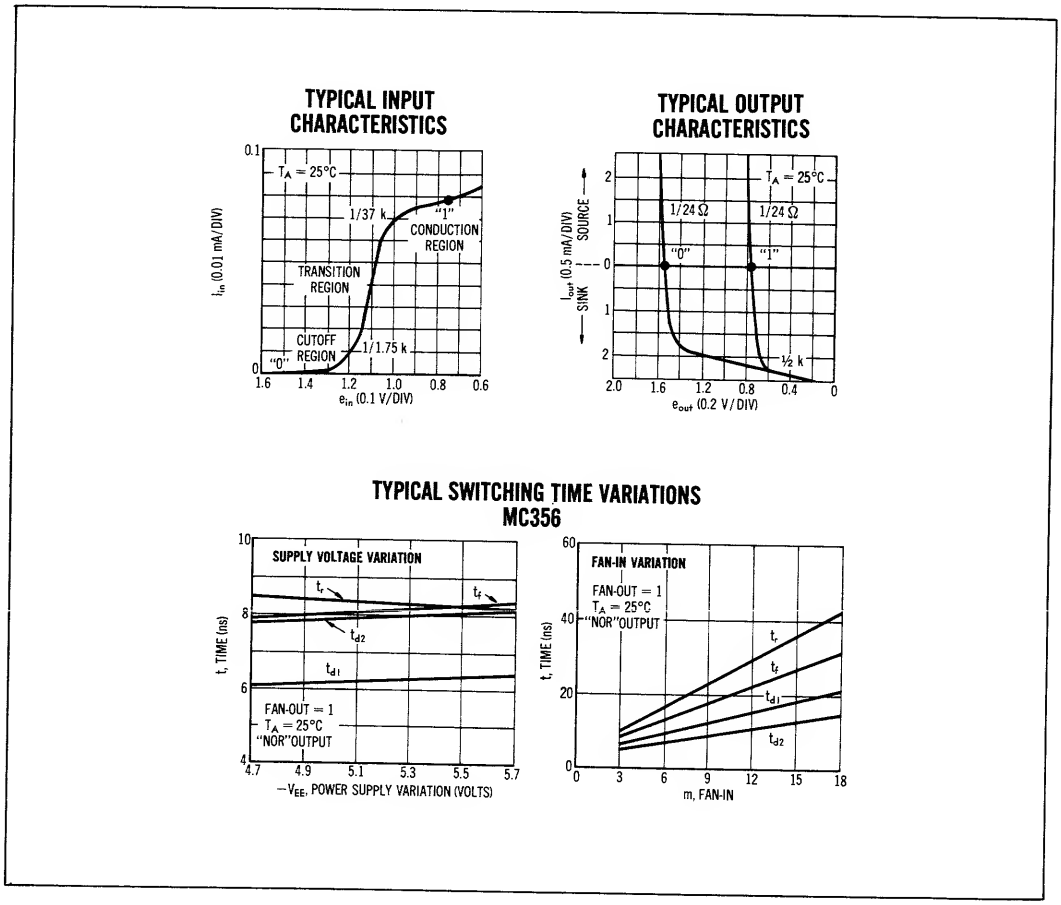
PROPAGATION DELAY



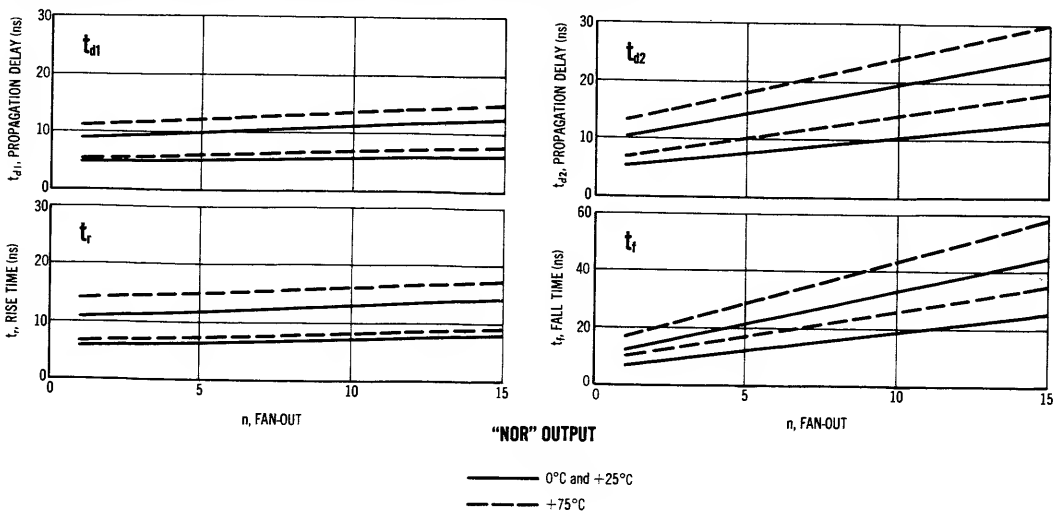
RISE AND FALL TIME



Fan-in obtained with MC355 input expanders; all but driven input connected to −5.2 V.



SWITCHING CHARACTERISTICS (10% to 90% distribution)



ELECTRICAL CHARACTERISTICS

	Test Conditions Vdc ±1%				
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08

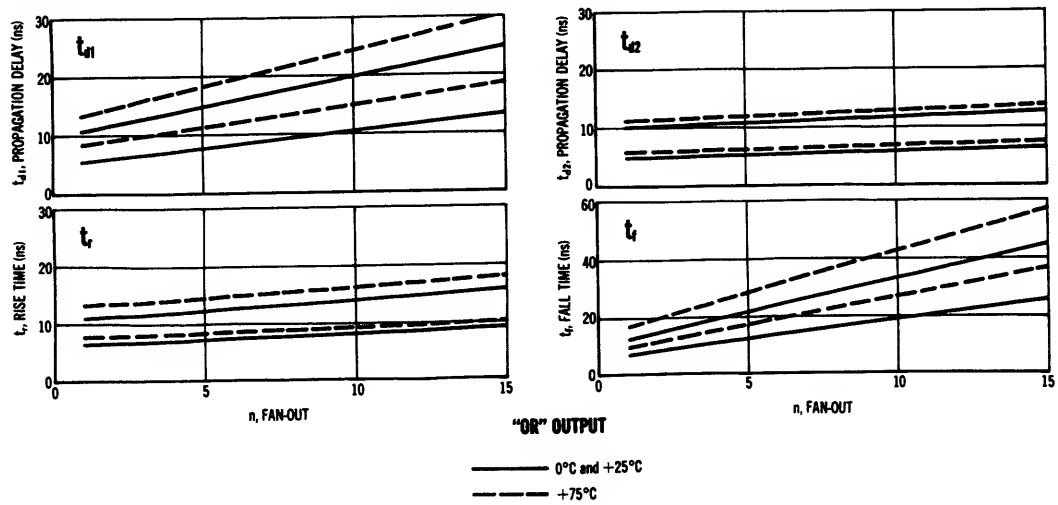
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{CC} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current MC356	—	—	—	2,6,7,6	1	—	—	3	I_E (2)	—	9.25	—	6.85	—	6.15	mAdc
Power Supply Drain Current MC357	—	—	—	2,6,7,8	1	—	—	3	I_E (2)	—	3.6	—	3.6	—	3.3	mAdc
Input Current	6	—	—	2,7,8	1	—	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	6	—	—	2,6,7	1	—	—	3	I_{in} (8)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	8	2,7,8	1	—	—	3	V_1 (5)	−0.715	−0.650	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	2,6,6	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	6	2,6,7	1	—	—	3	V_1 (5)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,6	1	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,6	1	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	—	—	3	V_4 (5)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	—	—	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	7	—	2,6,6	1	—	—	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	6	—	2,6,7	1	—	—	3	V_5 (4)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,6	1	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,6	1	—	—	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	6	2,6,7	1	—	—	3	V_2 (4)							
"NOR" Output Voltage Change (No load to full load)	—	—	8	2,7,6	1	—	5④	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
"OR" Output Voltage Change (No load to full load)	—	6	—	2,7,8	1	—	4④	3	ΔV_5 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,7,8	1	6①	—	3	V_3 (5)	—	− 0.51	—	− 0.55	—	− 0.63	Vdc
	—	—	—	2,6,8	1	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,6,7	1	8①	—	3	V_3 (5)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	8	4	—	2,7,8	1	—	—	3	t_{d1} (4)	8.5	11.5	8.5	11.5	10.0	15.0	ns
	6	5	—	2,7,8	1	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	4	—	2,7,8	1	—	—	3	t_{d2} (4)	6.0	11.0	6.0	11.0	7.5	12.0	
	6	5	—	2,7,8	1	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	4	—	2,7,6	1	—	—	3	t_r (4)	7.0	11.5	7.0	11.5	9.0	13.0	
	6	5	—	2,7,8	1	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	4	—	2,7,8	1	—	—	3	t_f (4)	9.0	14.0	9.5	14.0	12.0	17.0	
	6	5	—	2,7,8	1	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	

Pins not listed are left open

① Input voltage is adjusted to obtain dV "NOR" $/ dV_{in} = 0$.

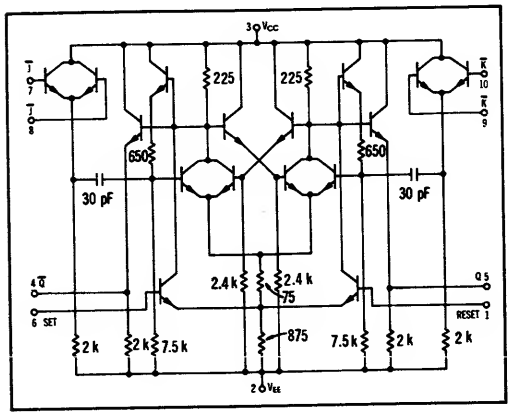
④ Current test conditions: no load = 0; full load = −2.5mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC358A

AC-coupled J-K flip-flop with dc Set and Reset inputs and buffered outputs for counter and shift register applications up to 15 MHz.



TRANSFER CHARACTERISTICS

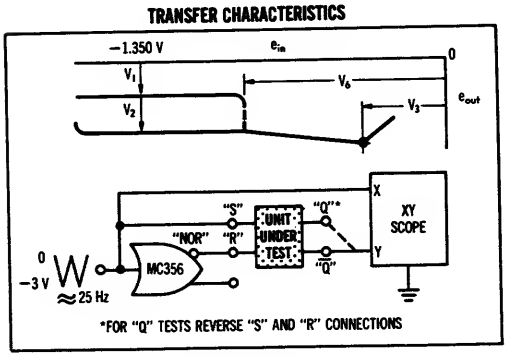


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

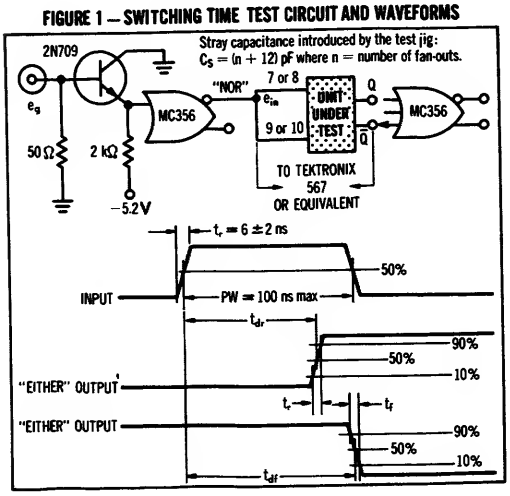


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

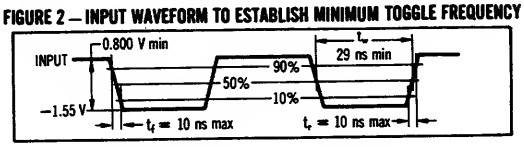


FIGURE 3 — SENSITIVITY (NO TOGGLE)

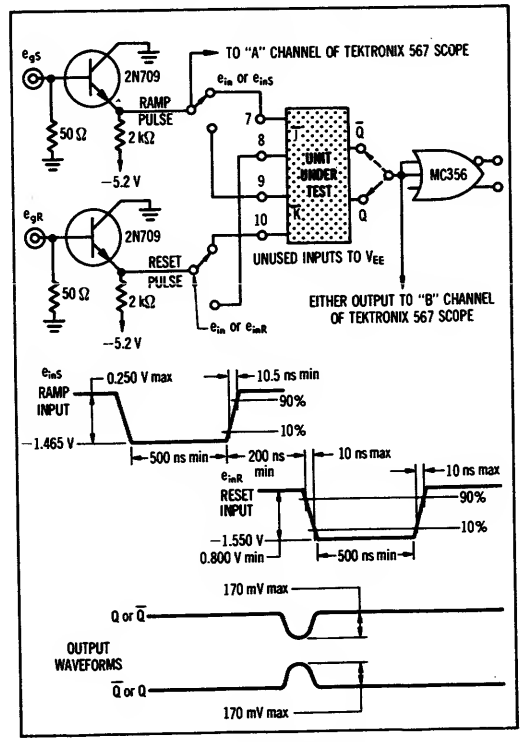
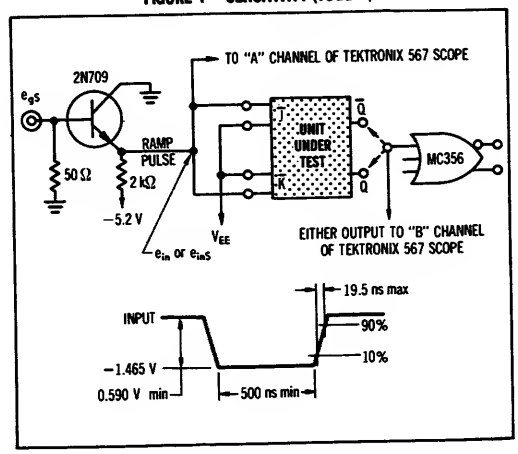


FIGURE 4 — SENSITIVITY (TOGGLE)



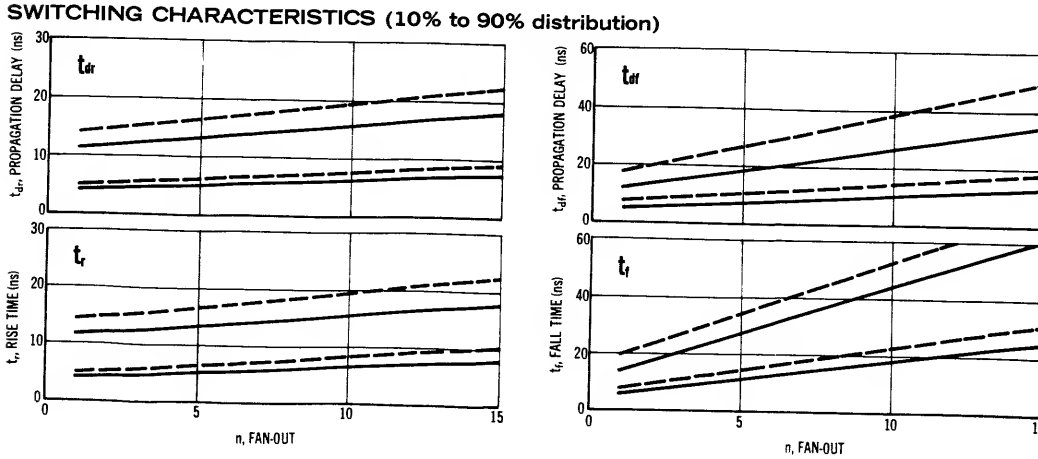
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{l\,max}$ Pin No	V_L ③ Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	22.0	—	21.0	—	19.6	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\bar{Q}$" Logical "1" Output Voltage	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\bar{Q}$" Logical "0" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5③	3	$\triangle V_1$ (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\bar{Q}$" Output Voltage Change	—	1	—	2,6,7,8,9,10	—	4③	3	$\triangle V_1$ (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	− 0.61	—	− 0.65	—	− 0.73	Vdc
"$\bar{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_2 (4)	—	− 0.61	—	− 0.65	—	− 0.73	Vdc
"Q" or "$\bar{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	− 1.11	− 1.25	− 1.09	− 1.21	−1.02	− 1.14	Vdc
	Pulse In	Pulse Out													
Toggle Frequency (See Figures 1 and 2)	7,10	5		1,2,6,9	—	—	3	f_{tog}	—	—	15	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4		1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5		1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggle)	7,10	4,5		1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	7,10	4,5		1,2,6,8,9	—	—	3	t_{dr} (4,5)	7.5	13.0	7.5	13.0	8.0	16.0	ns
	7,10	4,5		1,2,6,8,9	—	—	3	t_{df} (4,5)	10.0	14.5	10.0	15.0	11.0	20.0	
Rise Time	7,10	4,5		1,2,6,8,9	—	—	3	t_r (4,5)	8.0	13.0	8.0	13.0	8.5	16.0	↓
Fall Time	7,10	4,5		1,2,6,8,9	—	—	3	t_f (4,5)	10.5	15.5	11.0	15.5	12.5	22.0	

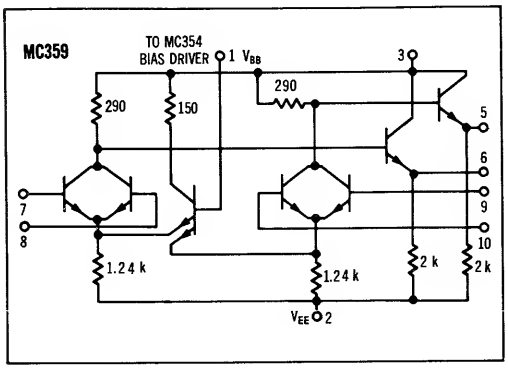
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = "0"$. ③ Current test conditions: no load = 0 to full load = −2.5 mAdc ±5%.
③ Apply momentary $V_{l\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

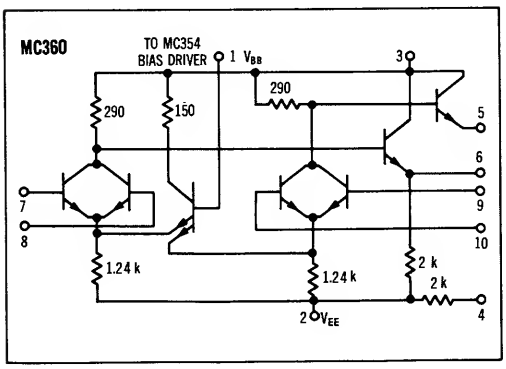
SWITCHING CHARACTERISTICS (10% to 90% distribution)

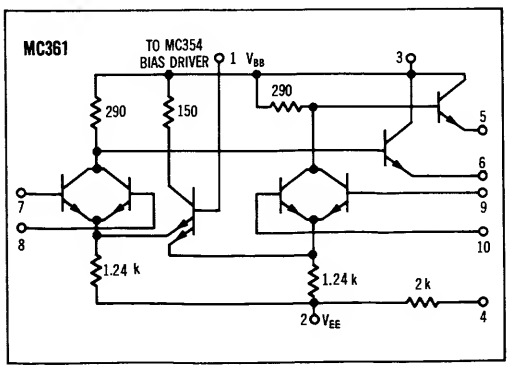


MC359 • MC360 • MC361

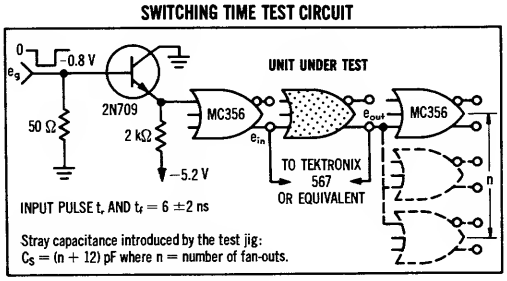
Dual 2-input gates that provide the positive logic "NOR" function. MC359 has two output pull-down resistors; MC360 has one of the output pull-down resistors optional; MC361 omits one output pull-down resistor and has the second optional.



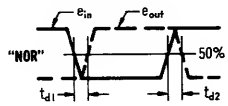




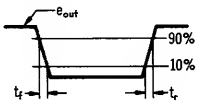
SWITCHING TIME TEST CIRCUIT



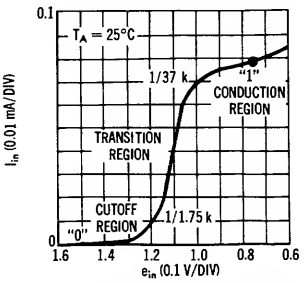
PROPAGATION DELAY



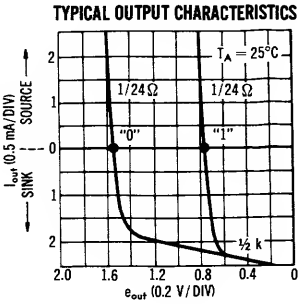
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



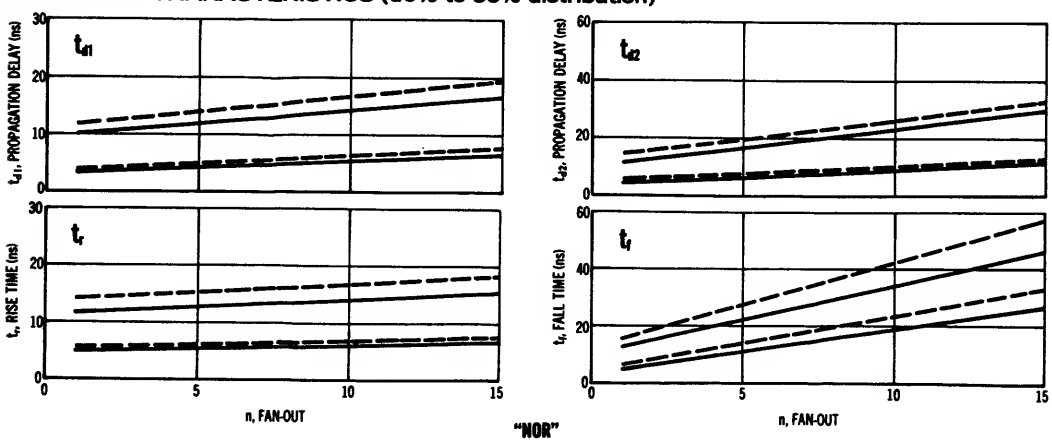
ELECTRICAL CHARACTERISTICS

Test Conditions Vdc ±1%					
@ Test Temperature	0°C	—	−0.850	−1.350	−5.20	−1.18
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
	+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Current MC359, MC360	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	13.55	—	13.0	—	12.0	mAdc
Drain Current MC361	—	—	—	2,7,8,9,10	1	—	—	3	I_E (2)	—	10.5	—	10.1	—	9.2	mAdc
Input Current	7	—	—	2,8,9,10	1	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	2,7,9,10	1	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	2,7,8,10	1	—	—	3	I_{in} (9)	—	—	—	↓	—	—	↓
	10	—	—	2,7,8,9	1	—	—	3	I_{in} (10)	—	—	—	↓	—	—	↓
"NOR" Logical "1" Output Voltage	—	—	7	2,8,9,10	1	—	—	3	V_1 (6)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	8	2,7,9,10	1	—	—	3	V_1 (6)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,7,8,10	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	10	2,7,8,9	1	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Logical "0" Output Voltage	—	7	—	2,8,9,10	1	—	—	3	V_0 (6)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	8	—	2,7,9,10	1	—	—	3	V_0 (6)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,7,8,10	1	—	—	3	V_0 (5)	↓	↓	↓	↓	↓	↓	↓
	—	10	—	2,7,8,9	1	—	—	3	V_0 (5)	↓	↓	↓	↓	↓	↓	↓
"NOR" Output Voltage Change (No load to full load)	—	—	—	2,7,8,9,10	1	—	6①	3	ΔV_1 (6)	—	−0.055	—	−0.055	—	−0.065	Vdc
	—	—	—	2,7,8,9,10	1	—	5①	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Vdc
"NOR" Saturation Breakpoint Voltage	—	—	—	2,8,9,10	1	7①	—	3	V_3 (6)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,7,9,10	1	8①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,10	1	9①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	2,7,8,9	1	10①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7	8	—	2,8,9,10	1	—	—	3	t_{d1} (6)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	10	5	—	2,7,8,9	1	—	—	3	t_{d1} (5)	6.5	11.0	8.5	11.0	8.0	14.5	↓
	7	6	—	2,8,9,10	1	—	—	3	t_{d0} (6)	8.5	13.5	8.5	13.5	10.0	16.0	↓
	10	5	—	2,7,8,9	1	—	—	3	t_{d0} (5)	8.5	13.5	8.5	13.5	10.0	16.0	↓
Rise Time	7	6	—	2,8,9,10	1	—	—	3	t_r (6)	8.5	12.5	9.0	12.5	11.0	15.5	↓
	10	5	—	2,7,8,9	1	—	—	3	t_r (5)	8.5	12.5	9.0	12.5	11.0	15.5	↓
Fall Time	7	6	—	2,8,9,10	1	—	—	3	t_f (6)	9.0	14.0	9.5	14.0	11.5	17.0	↓
	10	5	—	2,7,8,9	1	—	—	3	t_f (5)	9.0	14.0	9.5	14.0	11.5	17.0	↓

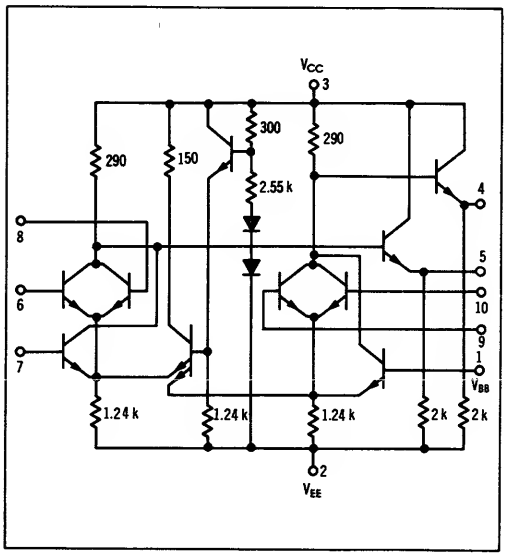
Pins not listed are left open For MC360, connect pin 4 to pin 5 for all tests ① Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0.
② Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

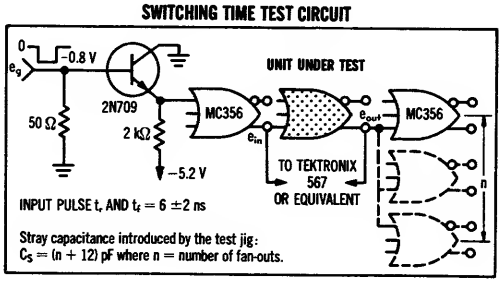


MC362A

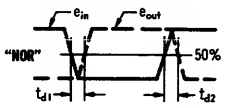
Dual 3-input gate that provides the positive logic "NOR" function, and features an internal bias driver. This gate is available without bias driver as MC362.



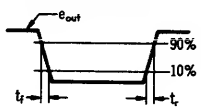
SWITCHING TIME TEST CIRCUIT



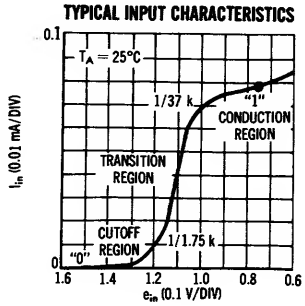
PROPAGATION DELAY



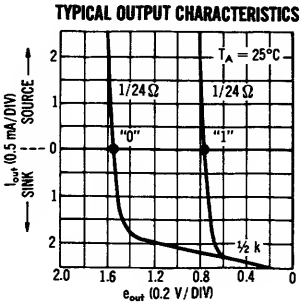
RISE AND FALL TIME



TYPICAL INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



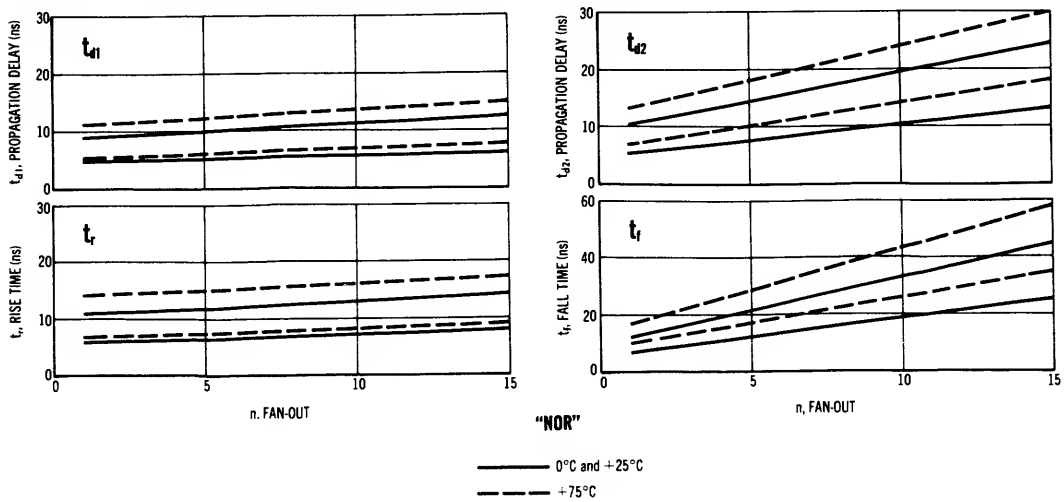
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,2,6,7,8,9,10	—	—	3	I_E (2)	—	17.7	—	17.0	—	16.4	mAdc
Input Current	1	—	—	2,6,7,8,9,10	—	—	3	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,2,7,8,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—		—	—	
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	6	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	7	1,2,6,8,9,10	—	—	3	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	1,2,6,7,9,10	—	—	3	V_1 (5)							
	—	—	1	2,6,7,8,9,10	—	—	3	V_1 (4)							
	—	—	9	1,2,6,7,8,10	—	—	3	V_1 (4)							
	—	—	10	1,2,6,7,8,9	—	—	3	V_1 (4)							
"NOR" Logical "0" Output Voltage	—	6	—	1,2,7,8,9,10	—	—	3	V_4 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	7	—	1,2,6,8,9,10	—	—	3	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	1,2,6,7,9,10	—	—	3	V_4 (5)							
	—	1	—	2,6,7,8,9,10	—	—	3	V_4 (4)							
	—	9	—	1,2,6,7,8,10	—	—	3	V_4 (4)							
	—	10	—	1,2,6,7,8,9	—	—	3	V_4 (4)							
"NOR" Output Voltage Change	—	—	6	1,2,7,8,9,10	—	5③	3	ΔV_1 (5)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	1	2,6,7,8,9,10	—	4③	3	ΔV_1 (4)	—	−0.055	—	−0.055	—	−0.065	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,2,6,8,9,10	7①	—	3	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,2,6,7,9,10	8①	—	3	V_3 (5)	—		—		—		
	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,10	9①	—	3	V_3 (4)	—		—		—		
	—	—	—	1,2,6,7,8,9	10①	—	3	V_3 (4)	—		—		—		
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	1,2,7,8,9,10	—	—	3	t_{d1} (5)	6.5	10.5	6.5	10.5	7.5	11.5	ns
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d1} (4)	6.5	10.5	6.5	10.5	7.5	11.5	↓
	6	5	—	1,2,7,8,9,10	—	—	3	t_{d2} (5)	8.5	11.5	8.5	11.5	10.0	15.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_{d2} (4)	8.5	11.5	8.5	11.5	10.0	15.0	
Rise Time	6	5	—	1,2,7,8,9,10	—	—	3	t_r (5)	9.0	12.5	9.5	12.5	11.5	15.5	
	1	4	—	2,6,7,8,9,10	—	—	3	t_r (4)	9.0	12.5	9.5	12.5	11.5	15.5	
Fall Time	6	5	—	1,2,7,8,9,10	—	—	3	t_f (5)	8.5	14.0	9.0	14.0	11.5	17.0	
	1	4	—	2,6,7,8,9,10	—	—	3	t_f (4)	8.5	14.0	9.0	14.0	11.5	17.0	↓

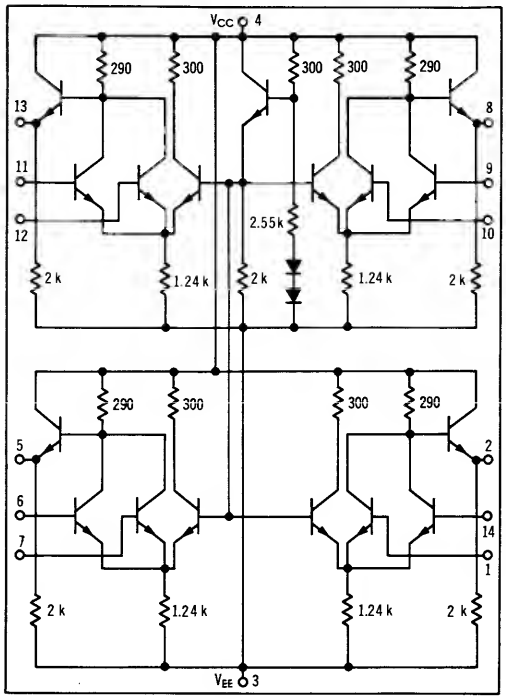
Pins not listed are left open.
① Input voltage is adjusted to obtain $dV_{"NOR"}/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

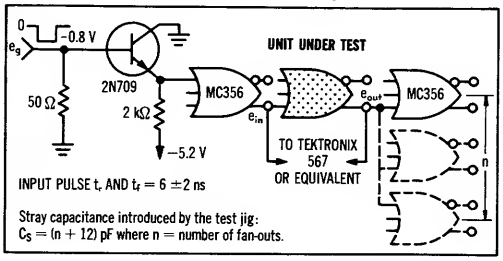


MC363F

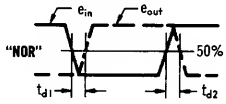
Quad 2-input gate that provides the positive logic "NOR" function, and features an internal bias driver.



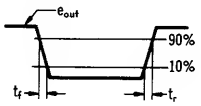
SWITCHING TIME TEST CIRCUIT



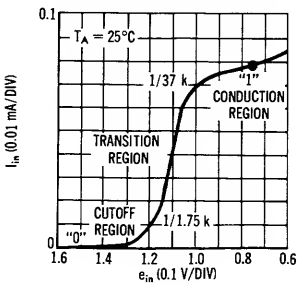
PROPAGATION DELAY



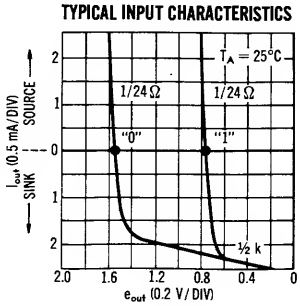
RISE AND FALL TIME



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL INPUT CHARACTERISTICS



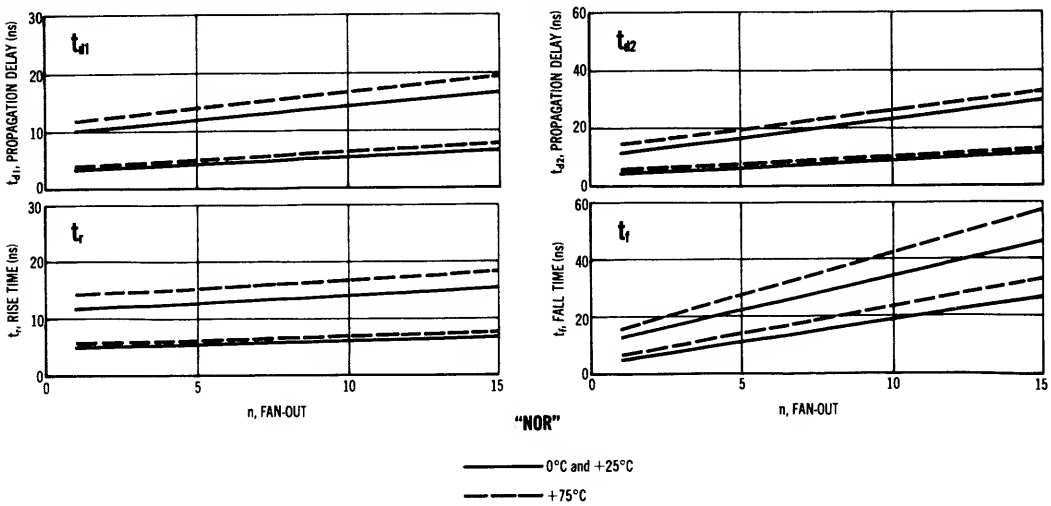
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ± 1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	1,3,6,7,9,10,11,12,14	—	—	4	I_E (3)	—	31.0	—	30.0	—	29.0	mAdc
Input Current	1	—	—	3,6,7,9,10,11,12,14	—	—	4	I_{in} (1)	—	—	—	100	—	—	μAdc
	6	—	—	1,3,7,9,10,11,12,14	—	—	4	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	1,3,6,9,10,11,12,14	—	—	4	I_{in} (7)	—	—	—		—	—	
	9	—	—	1,3,6,7,10,11,12,14	—	—	4	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,3,6,7,9,11,12,14	—	—	4	I_{in} (10)	—	—	—		—	—	
	11	—	—	1,3,6,7,9,10,12,14	—	—	4	I_{in} (11)	—	—	—		—	—	
	12	—	—	1,3,6,7,9,10,11,14	—	—	4	I_{in} (12)	—	—	—		—	—	
	14	—	—	1,3,6,7,9,10,11,12	—	—	4	I_{in} (14)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	1	3,6,7,9,10,11,12,14	—	—	4	V_1 (2)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
	—	—	6	1,3,7,9,10,11,12,14	—	—	4	V_1 (5)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	1,3,6,9,10,11,12,14	—	—	4	V_1 (5)							
	—	—	9	1,3,6,7,10,11,12,14	—	—	4	V_1 (8)							
	—	—	10	1,3,6,7,9,11,12,14	—	—	4	V_1 (8)							
	—	—	11	1,3,6,7,9,10,12,14	—	—	4	V_1 (13)							
	—	—	12	1,3,6,7,9,10,11,14	—	—	4	V_1 (13)							
	—	—	14	1,3,6,7,9,10,11,12	—	—	4	V_1 (2)							
"NOR" Logical "0" Output Voltage	—	1	—	3,6,7,9,10,11,12,14	—	—	4	V_4 (2)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
	—	6	—	1,3,7,9,10,11,12,14	—	—	4	V_4 (5)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	1,3,6,9,10,11,12,14	—	—	4	V_4 (5)							
	—	9	—	1,3,6,7,10,11,12,14	—	—	4	V_4 (8)							
	—	10	—	1,3,6,7,9,11,12,14	—	—	4	V_4 (8)							
	—	11	—	1,3,6,7,9,10,12,14	—	—	4	V_4 (13)							
	—	12	—	1,3,6,7,9,10,11,14	—	—	4	V_4 (13)							
	—	14	—	1,3,6,7,9,10,11,12	—	—	4	V_4 (2)							
"NOR" Output Voltage Change (No load to full load)	—	—	—	1,3,6,7,9,10,11,12,14	—	2⑤	4	ΔV_1 (2)	—	−0.055	—	−0.055	—	−0.065	Volts
	—	—	—	1,3,6,7,9,10,11,12,14	—	5⑤	4	ΔV_1 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,10,11,12,14	—	8⑤	4	ΔV_1 (8)	—		—		—		
	—	—	—	1,3,6,7,9,10,11,12,14	—	13⑤	4	ΔV_1 (13)	—		—		—		
"NOR" Saturation Breakpoint Voltage	—	—	—	3,6,7,9,10,11,12,14	1①	—	4	V_3 (2)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	1,3,6,9,10,11,12,14	7①	—	4	V_3 (5)	—	↓	—	↓	—	↓	↓
	—	—	—	1,3,6,7,9,11,12,14	10①	—	4	V_3 (8)	—		—		—		
	—	—	—	1,3,6,7,9,10,11,14	12①	—	4	V_3 (13)	—		—		—		
Switching Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d1} (2)	6.5	11.0	6.5	11.0	8.0	14.5	ns
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d1} (5)	↓	↓	↓	↓	↓	↓	↓
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d1} (8)							
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d1} (13)							
	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_{d2} (2)	8.5	13.5	8.5	13.5	10.0	16.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_{d2} (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_{d2} (8)							
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_{d2} (13)							
Rise Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_r (2)	8.5	12.5	9.0	12.5	11.0	15.5	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_r (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_r (8)							
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_r (13)							
Fall Time	1	2	—	3,6,7,9,10,11,12,14	—	—	4	t_f (2)	9.0	14.0	9.5	14.0	11.5	17.0	
	6	5	—	1,3,7,9,10,11,12,14	—	—	4	t_f (5)	↓	↓	↓	↓	↓	↓	
	9	8	—	1,3,6,7,10,11,12,14	—	—	4	t_f (8)							
	11	13	—	1,3,6,7,9,10,12,14	—	—	4	t_f (13)							

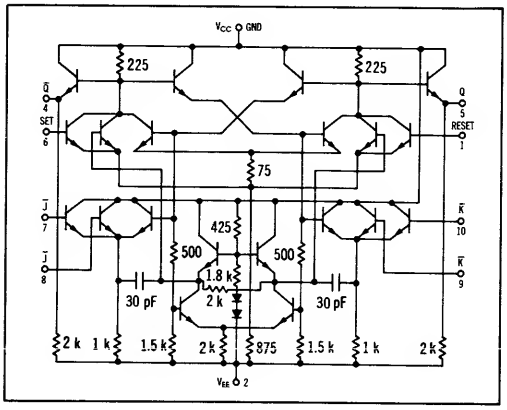
Pins not listed are left open. ① Input voltage is adjusted to obtain dV "NOR" / $dV_{in} = 0$. ⑤ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.

SWITCHING CHARACTERISTICS (10% to 90% distribution)



MC364

High-speed ac-coupled J-K flip-flop with dc Set and Reset input for counter and shift register applications up to 30 MHz operation.



TRANSFER CHARACTERISTICS

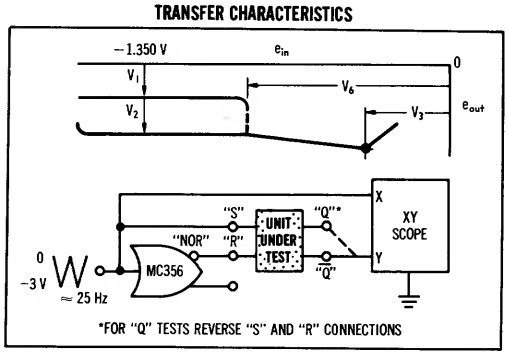


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

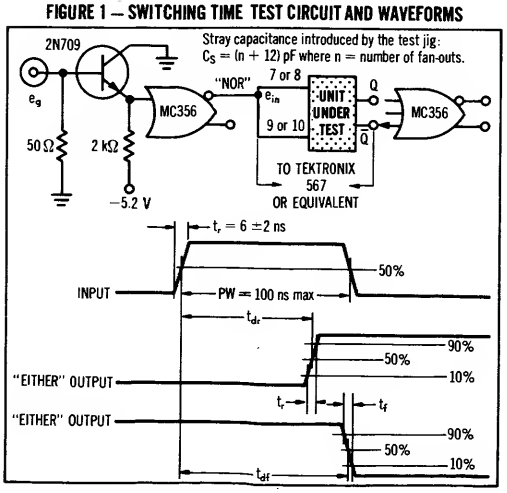


FIGURE 2 — INPUT WAVEFORM TO ESTABLISH MINIMUM TOGGLE FREQUENCY

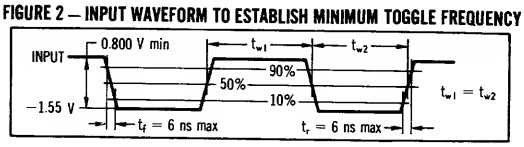


FIGURE 3 — SENSITIVITY (NO TOGGLE)

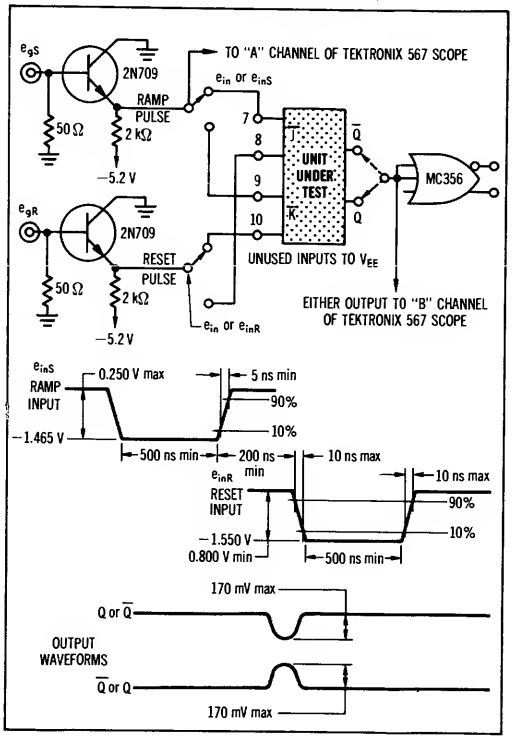
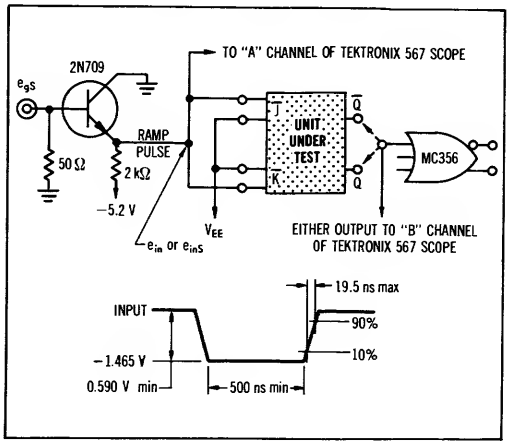


FIGURE 4 — SENSITIVITY (TOGGLE)



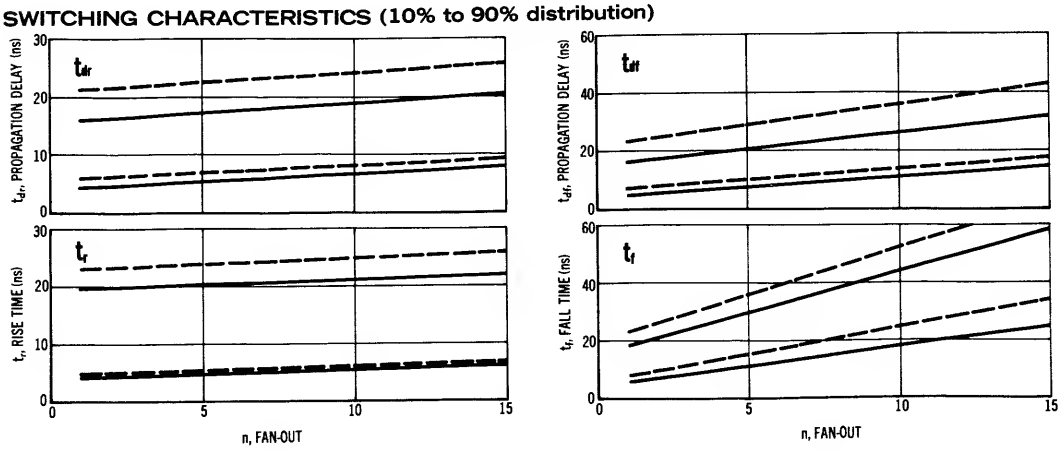
ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.350	−5.20
+25°C	−0.670	−0.795	−1.350	−5.20
+75°C	—	−0.725	−1.350	−5.20

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	7,10	—	1,2,6,8,9	—	—	3	I_E (2)	—	30.0	—	28.5	—	28.0	mAdc
Input Current	7	—	—	1,2,6,8,9,10	—	—	3	I_{in} (7)	—	—	—	100	—	—	μAdc
	8	—	—	1,2,6,7,9,10	—	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
	9	—	—	1,2,6,7,8,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	1,2,6,7,8,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"Q" Logical "1" Output Voltage	—	—	6⑤	1,2,7,8,9,10	—	—	3	V_1 (5)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"Q" Logical "0" Output Voltage	—	—	1⑤	2,6,7,8,9,10	—	—	3	V_2 (5)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"$\overline{Q}$" Logical "1" Outpnt Vnltage	—	—	1⑤	2,6,7,8,9,10	—	—	3	V_1 (4)	−0.715	−0.850	−0.670	−0.795	−0.590	−0.725	Vdc
"$\overline{Q}$" Logical "0" Outpnt Voltage	—	—	6⑤	1,2,7,8,9,10	—	—	3	V_2 (4)	−1.510	−1.880	−1.465	−1.750	−1.395	−1.730	Vdc
"Q" Output Voltage Change	—	6	—	1,2,7,8,9,10	—	5⑤	3	$\triangle V_1$ (5)	—	−0.065	—	−0.065	—	−0.075	Volts
"$\overline{Q}$" Output Voltage Cnnoge	—	1	—	2,6,7,8,9,10	—	4⑤	3	$\triangle V_1$ (4)	—	−0.065	—	−0.065	—	−0.075	Volts
"Q" Saturation Brenkpoint Voltage	—	—	—	1,2,7,8,9,10	6①	—	3	V_3 (5)	—	−0.61	—	−0.65	—	−0.73	Vdc
"$\overline{Q}$" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,9,10	1①	—	3	V_3 (4)	—	−0.61	—	−0.65	—	−0.73	Vdc
"Q" or "$\overline{Q}$" Latch Voltage	—	—	—	2,7,8,9,10	1,6④	—	3	V_4 (1,6)	−1.11	−1.25	−1.09	−1.21	−1.02	−1.14	Vdc
	Pulse In	Pulse Out													
Toggin Frequency (See Figures 1 and 2)	7,10	5	—	1,2,6,9	—	—	3	f_{reg}	—	—	30	—	—	—	MHz
Sensitivity (No Toggle)	7,10	4	—	1,2,6,8,9	—	—	3	← See Figure 3 →							
	8,9	5	—	1,2,6,7,10	—	—	3	← See Figure 3 →							
Sensitivity (Toggin)	7,10	4,5	—	1,2,6,8,9	—	—	3	← See Figure 4 →							
Switching Times									Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{dr} (4,5)	11.0	18.0	12.0	18.0	14.0	24.0	ns
	7,10	4,5	—	1,2,6,8,9	—	—	3	t_{df} (4,5)	12.0	18.0	13.0	18.0	15.0	24.0	
Rise Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_r (4,5)	11.5	20.0	12.5	21.0	15.0	26.0	↓
Fnll Time	7,10	4,5	—	1,2,6,8,9	—	—	3	t_f (4,5)	11.5	18.0	12.5	21.0	15.0	26.0	

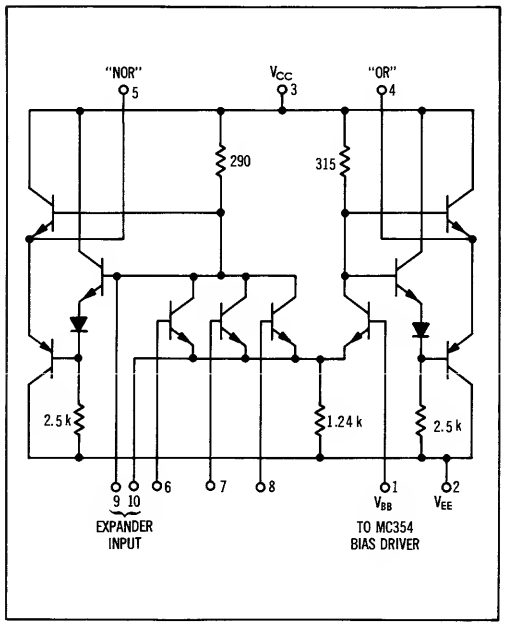
Pins not listed are left open. ① Input voltage is adjusted to obtain $dV_{out}/dV_{in} = 0$. ③ Current test conditions: no load = 0; full load = −2.5 mAdc ±5%.
⑤ Apply momentary $V_{I\,max}$ to set output, then V_{in} for measurement. ④ Input voltage is adjusted to obtain $dV_1/dV_{in} = \infty$.

SWITCHING CHARACTERISTICS (10% to 90% distribution)

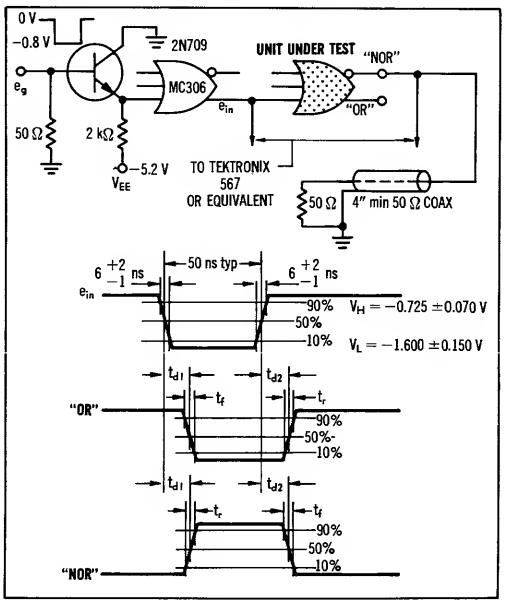


MC365

Line driver for driving lines of 50 ohms or greater while providing the positive logic "NOR" function and its complement simultaneously.



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

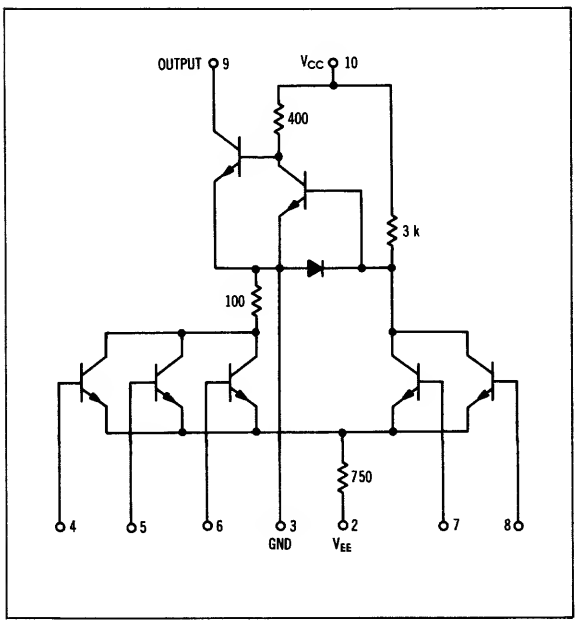
		Test Conditions Vdc ±1%				
@ Test Temperature	0°C	—	−0.850	−1.350	−5.20	−1.18
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15
	+75°C	—	−0.725	−1.350	−5.20	−1.08

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	I_L① Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,6,7,8	1	4,5	3	I_E (2)	—	68	—	65	—	63	mAdc
Input Current	6	—	—	2,7,8	1	—	3	I_{in} (6)	—	—	—	100	—	—	μAdc
	7	—	—	2,6,8	1	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,6,7	1	—	3	I_{in} (8)	—	—	—	—	—	—	
"NOR" Logical "1" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_1 (6)	−0.695	−0.850	−0.650	−0.795	−0.570	−0.725	Vdc
	—	—	7	2,6,8	1	4,5	3	V_1 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_1 (8)							
"NOR" Logical "0" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_4 (6)	−1.495	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	—	7	—	2,6,8	1	4,5	3	V_4 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_4 (8)							
"OR" Logical "1" Output Voltage	—	6	—	2,7,8	1	4,5	3	V_2 (6)	−0.695	−0.850	−0.650	−0.795	−0.570	−0.725	Vdc
	—	7	—	2,6,8	1	4,5	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	8	—	2,6,7	1	4,5	3	V_2 (8)							
"OR" Logical "0" Output Voltage	—	—	6	2,7,8	1	4,5	3	V_5 (6)	−1.495	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	—	—	7	2,6,8	1	4,5	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	8	2,6,7	1	4,5	3	V_5 (8)							
Switching Times	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	6	5	—	2,7,8	1	—	3	t_{d1} (5)	12.0	20.0	12.0	20.0	13.5	25.0	ns
	6	4	—	2,7,8	1	—	3	t_{d1} (4)	16.0	25.0	16.0	25.0	18.5	30.0	↓
	6	5	—	2,7,8	1	—	3	t_{d2} (5)	14.0	25.0	14.0	25.0	16.0	30.0	
	6	4	—	2,7,8	1	—	3	t_{d2} (4)	10.0	20.0	10.0	20.0	11.0	23.0	
Rise Time	6	5	—	2,7,8	1	—	3	t_r (5)	16.5	25.0	16.0	25.0	19.0	30.0	
	6	4	—	2,7,8	1	—	3	t_r (4)	13.0	20.0	13.0	20.0	15.5	25.0	
Fall Time	6	5	—	2,7,8	1	—	3	t_f (5)	20.5	35.0	20.5	35.0	26.0	47.0	
	6	4	—	2,7,8	1	—	3	t_f (4)	20.0	35.0	20.0	35.0	23.0	47.0	↓

Pins not listed are left open. ①Output is loaded with a 50-ohm resistor.

MC366

Lamp driver that provides "OR" or "NOR" logic depending on the bias arrangement used and is capable of driving 6V lamps.



ELECTRICAL CHARACTERISTICS

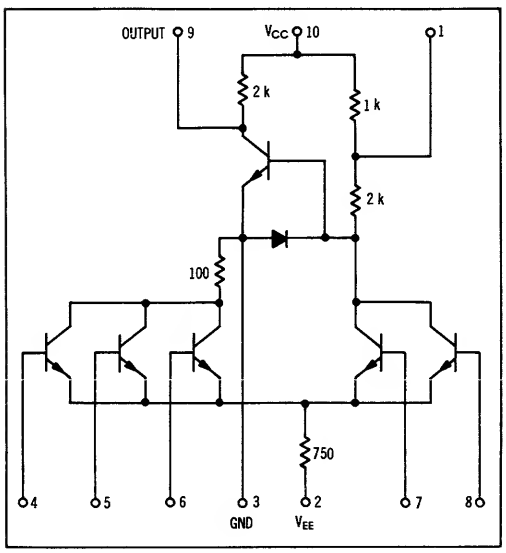
	Test Conditions						
	Vdc ±1%						mAdc
@ Test Temperature 0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	100
@ Test Temperature +25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	100
@ Test Temperature +75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	100

Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	4,5,6	—	2,7	8	10	—	3	I_C (10)	—	22.5	—	21.5	—	20.7	mAdc
	—	4,5,6	—	2,7	8	10	—	3	I_E (2)	—	8.4	—	8.0	—	7.7	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,4,5,6	8	10	—	3	I_{in} (7)	—	—	—	↓	—	—	↓
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—	↓	—	—	↓
Output Voltage, Low	—	—	6	2,4,5,7	8	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
	—	—	6	2,4,5,8	7	10	9	3	V_{OL} (9)	—	0.9	—	1.0	—	1.25	Vdc
Output Voltage, High	—	4	—	2,5,6,7	8	10,9①	—	3	V_{OH} (4)	—	—	—	5.8	—	5.8	Vdc
	—	5	—	2,4,6,7	8	10,9①	—	3	V_{OH} (5)	—	—	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—	↓	↓
	—	6	—	2,4,5,8	7	10,9①	—	3	V_{OH} (6)	—	—	—	↓	—	↓	↓

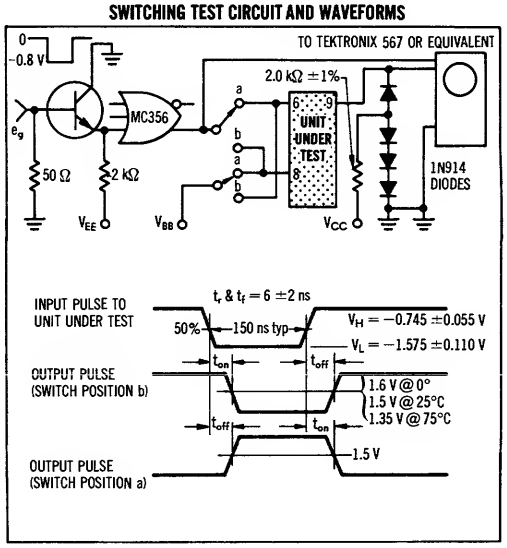
Pins not listed are left open. ①Pin 9 is connected to V_{CC} through a 10 k-ohm resistor.

MC367

Level translator intended for converting non-saturated MECL signal levels to saturated logic levels; provides "OR" or "NOR" logic depending on the bias arrangement used.



SWITCHING TEST CIRCUIT AND WAVEFORMS



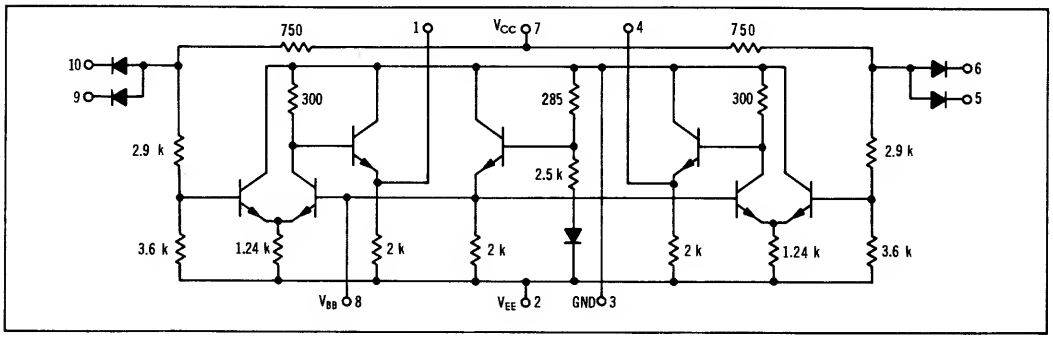
ELECTRICAL CHARACTERISTICS

		Test Conditions						
		Vdc ±1%						mAdc
@ Test Temperature	0°C	—	−0.850	−1.350	−5.20	−1.18	+6.0	10
	+25°C	−0.670	−0.795	−1.350	−5.20	−1.15	+6.0	10
	+75°C	—	−0.725	−1.350	−5.20	−1.08	+6.0	10

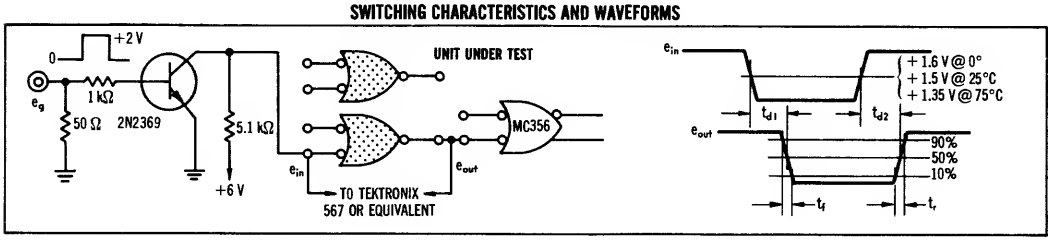
Characteristic	V_H Pin No	$V_{I\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	V_{BB} Pin No	V_{CC} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	6	—	2,4,5,7	8	10	—	3	I_C (10)	—	7.3	—	7.0	—	6.8	mAdc
	—	—	—	2,4,5,6,7	8	10	—	3	I_E (2)	—	7.3	—	7.0	—	6.8	mAdc
Input Current	4	—	—	2,5,6,7	8	10	—	3	I_{in} (4)	—	—	—	200	—	—	μAdc
	5	—	—	2,4,6,7	8	10	—	3	I_{in} (5)	—	—	—	↓	—	—	↓
	6	—	—	2,4,5,7	8	10	—	3	I_{in} (6)	—	—	—		—	—	
	7	—	—	2,4,5,8	6	10	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,4,5,7	6	10	—	3	I_{in} (8)	—	—	—		—	—	
Output Voltage, High	—	—	—	2,4,5,6,7	8	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
	—	—	—	2,4,5,6,8	7	10	—	3	V_{OH} (9)	—	—	5.8	—	—	—	Vdc
Output Voltage, Low	—	4	—	2,5,6,7	8	10	9	3	V_{OL} (9)	—	0.45	—	0.45	—	0.50	Vdc
	—	5	—	2,4,6,7	8	10	9	3	V_{OL} (9)	—	↓	—	↓	—	↓	↓
	—	6	—	2,4,5,7	8	10	9	3	V_{OL} (9)	—		—		—		
	—	6	—	2,4,5,8	7	10	9	3	V_{OL} (9)	—		—		—		
Switching Times	Pulse In	Pulse Out								Typ	Max	Typ	Max	Typ	Max	
Turn-On Time	6	9	—	2,4,5,7	8	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	ns
	8	9	—	2,4,5,7	6	10	—	3	t_{on} (9)	27.5	40.0	27.5	40.0	29.5	43.0	↓
Turn-Off Time	6	9	—	2,4,5,7	8	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	
	8	9	—	2,4,5,7	6	10	—	3	t_{off} (9)	25.0	40.0	26.0	40.0	27.0	43.0	

MC368

Level translator intended for converting saturated logic levels to non-saturated MECL signal levels.



SWITCHING CHARACTERISTICS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS

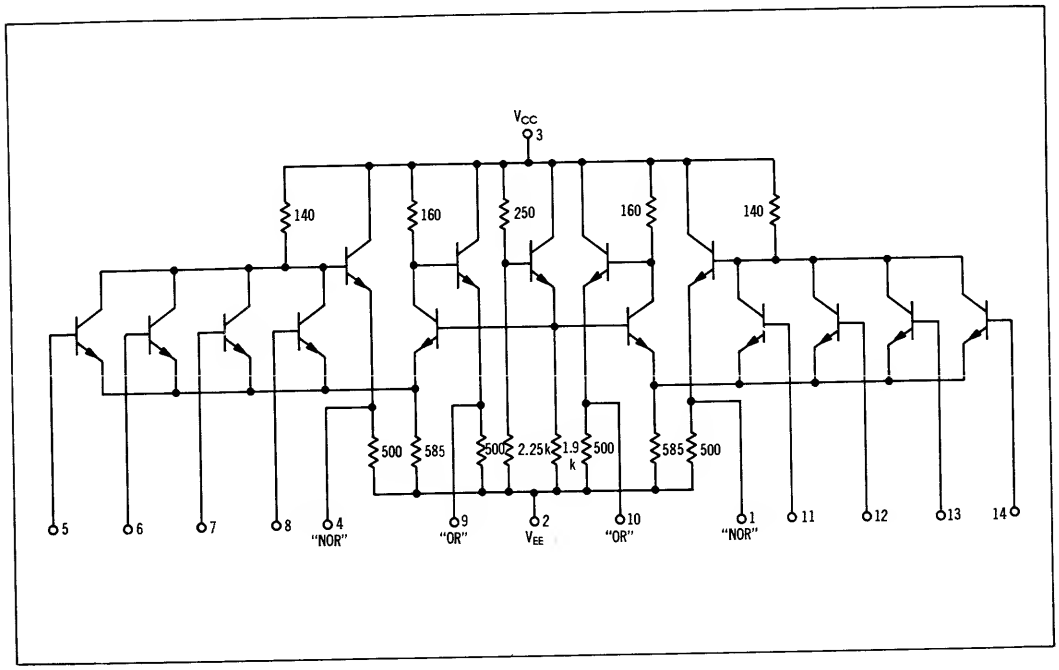
		Test Conditions Vdc ±1%			
@ Test Temperature	0°C	+0.45	+5.0	−5.20	+6.0
	+25°C	+0.45	+5.0	−5.20	+6.0
	+75°C	+0.50	+5.0	−5.20	+6.0

Characteristic	V_{IL} Pin No	V_{IH} Pin No	V_{EE} Pin No	V_{CC} Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	2	7	3	I_C (7)	—	4.2	—	4.0	—	3.9	mAdc
	—	—	2	7	3	I_E (2)	—	21.9	—	21.0	—	20.2	mAdc
Input Load Current	—	—	2	7	3,5	I_L (5)	—	—	—	8.5	—	—	mAdc
	—	—	2	7	3,6	I_L (6)	—	—	—	↓	—	—	↓
	—	—	2	7	3,9	I_L (9)	—	—	—		—	—	
	—	—	2	7	3,10	I_L (10)	—	—	—		—	—	
Input Reverse Current	—	—	2	5,7	3,6	I_R (5)	—	—	—	0.5	—	2.0	μAdc
	—	—	2	6,7	3,5	I_R (6)	—	—	—	↓	—	↓	↓
	—	—	2	7,9	3,10	I_R (9)	—	—	—		—		
	—	—	2	7,10	3,9	I_R (10)	—	—	—		—		
"OR" Logical "1" Output Voltage	—	5	2	7	3	V_5 (4)	−0.715	−0.850	−0.670	−0.795	−0.570	−0.725	Vdc
	—	6	2	7	3	V_5 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	2	7	3	V_5 (1)							
	—	10	2	7	3	V_5 (1)							
"OR" Logical "0" Output Voltage	5	—	2	7	3	V_2 (4)	−1.510	−1.880	−1.450	−1.750	−1.395	−1.730	Vdc
	6	—	2	7	3	V_2 (4)	↓	↓	↓	↓	↓	↓	↓
	9	—	2	7	3	V_2 (1)							
	10	—	2	7	3	V_2 (1)							
Bias Voltage Output	—	—	2	7	3	V_{BB} (8)	−1.14	−1.27	−1.09	−1.22	−1.04	−1.18	Vdc
Switching Times	Pulse In	Pulse Out					Typ	Max	Typ	Max	Typ	Max	
Propagation Delay Time	5	4	2	7	3	t_{d1} (4)	14.5	24.0	15.0	24.0	19.0	28.0	ns
	9	1	2	7	3	t_{d1} (1)	14.5	24.0	15.0	24.0	19.0	28.0	↓
	5	4	2	7	3	t_{d2} (4)	15.5	23.0	15.5	23.0	19.0	28.0	
	9	1	2	7	3	t_{d2} (1)	15.5	23.0	15.5	23.0	19.0	28.0	
Rise Time	5	4	2	7	3	t_r (4)	6.5	13.0	7.0	13.0	8.0	14.0	
	9	1	2	7	3	t_r (1)	6.5	13.0	7.0	13.0	8.0	14.0	
Fall Time	5	4	2	7	3	t_f (4)	7.0	13.0	7.5	13.0	8.0	14.0	
	9	1	2	7	3	t_f (1)	7.0	13.0	7.5	13.0	8.0	14.0	↓

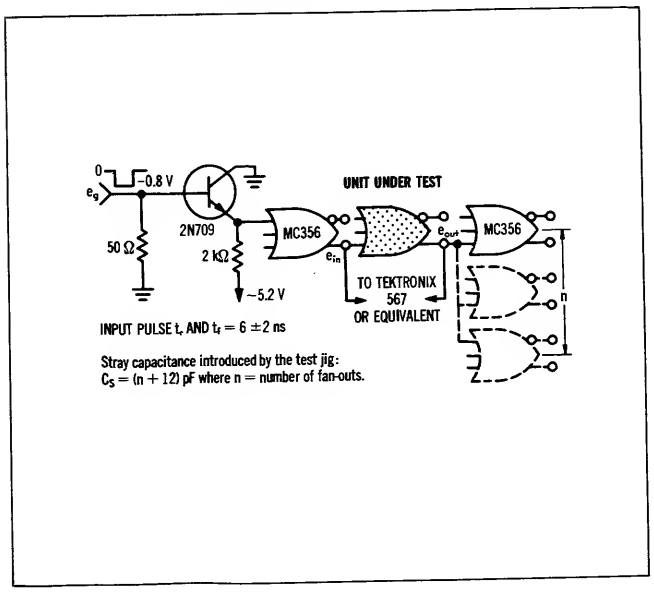
Pins not listed are left open.

MC369F

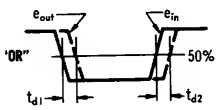
High-speed clock driver or dual 4-input gate that provides the positive logic "NOR" function and its complement simultaneously.

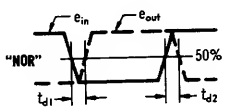


SWITCHING TIME TEST CIRCUIT

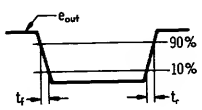


PROPAGATION DELAY





RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

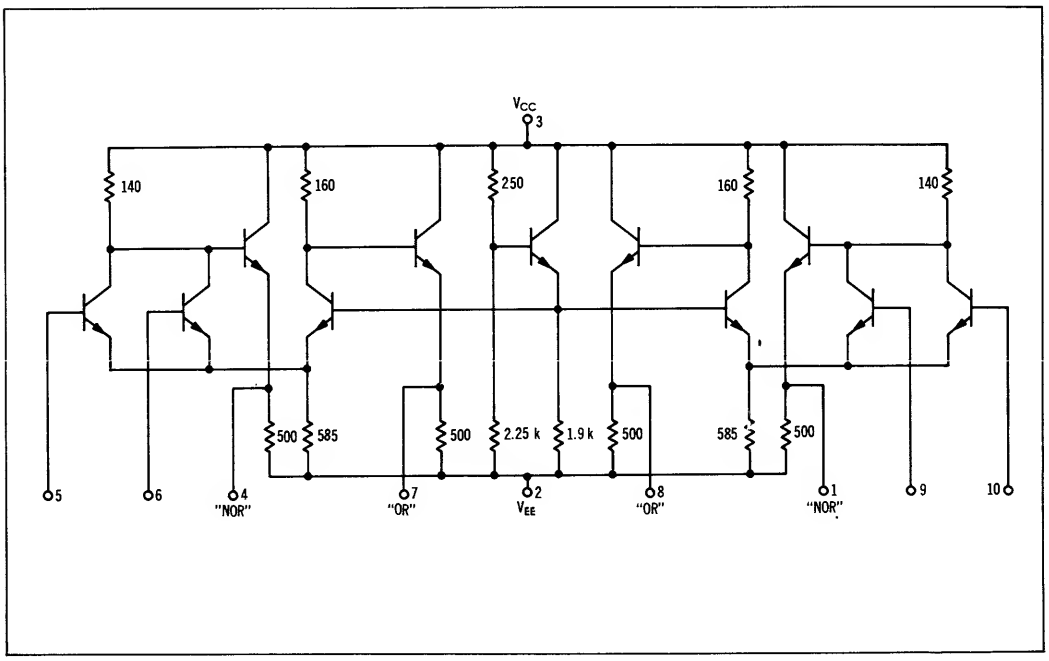
@ Test Temperature	Test Conditions Vdc ±1%			
0°c	—	−0.850	−1.510	−5.20
+25°c	−0.670	−0.795	−1.465	−5.20
+75°c	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{t\,max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,5,6,7,8,11,12,13,14	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,7,8,11,12,13,14	—	—	3	I_{in} (5)	—	—	—	200	—	—	μAdc
	6	—	—	2,5,7,8,11,12,13,14	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	7	—	—	2,5,6,8,11,12,13,14	—	—	3	I_{in} (7)	—	—	—		—	—	
	8	—	—	2,5,6,7,11,12,13,14	—	—	3	I_{in} (8)	—	—	—		—	—	
	11	—	—	2,5,6,7,8,12,13,14	—	—	3	I_{in} (11)	—	—	—		—	—	
	12	—	—	2,5,6,7,8,11,13,14	—	—	3	I_{in} (12)	—	—	—		—	—	
	13	—	—	2,5,6,7,8,11,12,14	—	—	3	I_{in} (13)	—	—	—		—	—	
	14	—	—	2,5,6,7,8,11,12,13	—	—	3	I_{in} (14)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	—	6	2,5,7,8,11,12,13,14	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_1 (4)							
	—	—	8	2,5,6,7,11,12,13,14	—	—	3	V_1 (4)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_1 (1)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_1 (1)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_1 (1)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_1 (1)							
"NOR" Logical "0" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_4 (4)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_4 (4)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_4 (4)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_4 (1)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_4 (1)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_4 (1)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_4 (1)							
"OR" Logical "1" Output Voltage	—	5	—	2,6,7,8,11,12,13,14	—	—	3	V_5 (9)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,7,8,11,12,13,14	—	—	3	V_5 (9)	↓	↓	↓	↓	↓	↓	↓
	—	7	—	2,5,6,8,11,12,13,14	—	—	3	V_5 (9)							
	—	8	—	2,5,6,7,11,12,13,14	—	—	3	V_5 (9)							
	—	11	—	2,5,6,7,8,12,13,14	—	—	3	V_5 (10)							
	—	12	—	2,5,6,7,8,11,13,14	—	—	3	V_5 (10)							
	—	13	—	2,5,6,7,8,11,12,14	—	—	3	V_5 (10)							
	—	14	—	2,5,6,7,8,11,12,13	—	—	3	V_5 (10)							
"OR" Logical "0" Output Voltage	—	—	5	2,6,7,8,11,12,13,14	—	—	3	V_2 (9)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	—	6	2,5,7,8,11,12,13,14	—	—	3	V_2 (9)	↓	↓	↓	↓	↓	↓	↓
	—	—	7	2,5,6,8,11,12,13,14	—	—	3	V_2 (9)							
	—	—	8	2,5,6,7,11,12,13,14	—	—	3	V_2 (9)							
	—	—	11	2,5,6,7,8,12,13,14	—	—	3	V_3 (10)							
	—	—	12	2,5,6,7,8,11,13,14	—	—	3	V_3 (10)							
	—	—	13	2,5,6,7,8,11,12,14	—	—	3	V_3 (10)							
	—	—	14	2,5,6,7,8,11,12,13	—	—	3	V_3 (10)							
"NOR" Output Voltage Change	—	—	5	2,6,7,8,11,12,13,14	—	4③	3	ΔV_1 (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	11	2,5,6,7,8,12,13,14	—	1③	3	ΔV_1 (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" Output Voltage Change	—	5	—	2,6,7,8,11,12,13,14	—	9③	3	ΔV_5 (9)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	11	—	2,5,6,7,8,12,13,14	—	10③	3	ΔV_5 (10)	—	−0.100	—	−0.100	—	−0.130	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,7,8,11,12,13,14	5①	—	3	V_3 (5)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2 5,7,8,11,12,13,14	6①	—	3	V_3 (6)	—	↓	—	↓	—	↓	↓
	—	—	—	2 5,6,8,11,12,13,14	7①	—	3	V_3 (7)	—		—		—		
	—	—	—	2,5,6,7,11,12,13,14	8①	—	3	V_3 (8)	—		—		—		
	—	—	—	2,5,6,7,8,12,13,14	11①	—	3	V_3 (11)	—		—		—		
	—	—	—	2,5,6,7,8,11,13,14	12①	—	3	V_3 (12)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,14	13①	—	3	V_3 (13)	—		—		—		
	—	—	—	2,5,6,7,8,11,12,13	14①	—	3	V_3 (14)	—		—		—		
Switching Times Propagation Delay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d1} (9)		6		6		7	↓
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)		5		5		6	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (10)	↓	6	↓	6	↓	7	
	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	3	6	3	6	4	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (9)		5		5		6	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)		6		6		7	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)	↓	5	↓	5	↓	6	
Fan-Out = 10	5	4	—	2 6,7,8,11,12,13,14	—	—	3	t_{d1} (4)	4	7	4	7	5	8	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_{d1} (9)	5	10	5	10	6	11	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d1} (1)	4	7	4	7	5	8	
	11	10	—	2,5,6 7,8,12,13,14	—	—	3	t_{d1} (10)	5	10	5	10	6	11	
	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_{d2} (4)	5	10	5	10	6	11	
	5	9	—	2 6,7,8,11,12,13,14	—	—	3	t_{d2} (9)	4	7	4	7	5	8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (1)	5	10	5	10	6	11	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_{d2} (10)	4	7	4	7	5	8	
Rise Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	7	4	7	5	9	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_r (9)		6		6		8	
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)		7		7		9	
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)	↓	6	↓	6	↓	8	
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_r (4)	4	9	4	9	5	10	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_r (9)							
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_r (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_r (10)	↓	↓	↓	↓	↓	↓	
Fall Time, Fan-Out = 1	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	4	6	4	6	5	7	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)							
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)	↓	↓	↓	↓	↓	↓	
Fan-Out = 10	5	4	—	2,6,7,8,11,12,13,14	—	—	3	t_f (4)	6	11	6	11	7	12	
	5	9	—	2,6,7,8,11,12,13,14	—	—	3	t_f (9)							
	11	1	—	2,5,6,7,8,12,13,14	—	—	3	t_f (1)							
	11	10	—	2,5,6,7,8,12,13,14	—	—	3	t_f (10)	↓	↓	↓	↓	↓	↓	

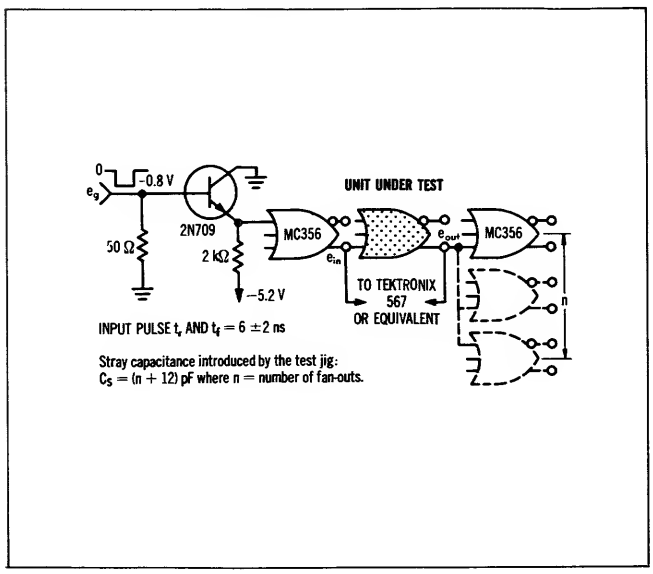
Pins not listed are left open. ①Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ③Current test conditions: no load = 0; full load = −10 mAdc ±5%.

MC369G

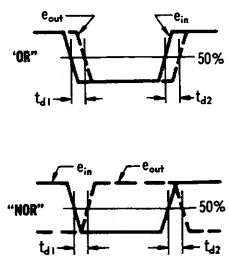
High-speed clock driver or dual 2-input gate that provides the positive logic "NOR" function and its complement simultaneously.



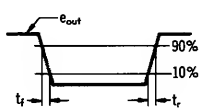
SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY



RISE AND FALL TIME



ELECTRICAL CHARACTERISTICS

@ Test Temperature	Test Conditions Vdc ±1%			
0°C	—	−0.850	−1.510	−5.20
+25°C	−0.670	−0.795	−1.465	−5.20
+75°C	—	−0.725	−1.395	−5.20

Characteristic	V_H Pin No	$V_{I\ max}$ Pin No	V_L Pin No	V_{EE} Pin No	dV_{in} Pin No	I_L Pin No	Ground Pin No	Symbol Pin No in ( )	Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	—	—	—	2,5,6,9,10	—	—	3	I_E (2)	—	—	—	60	—	—	mAdc
Input Current	5	—	—	2,6,9,10	—	—	3	I_{in} (5)	—	—	—	200	—	—	μAdc
	6	—	—	2,5,9,10	—	—	3	I_{in} (6)	—	—	—	↓	—	—	↓
	9	—	—	2,5,6,10	—	—	3	I_{in} (9)	—	—	—		—	—	
	10	—	—	2,5,6,9	—	—	3	I_{in} (10)	—	—	—		—	—	
"NOR" Logical "1" Output Voltage	—	—	5	2,6,9,10	—	—	3	V_1 (4)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	—	6	2,5,9,10	—	—	3	V_1 (4)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_1 (1)							
	—	—	10	2,5,6,9	—	—	3	V_1 (1)							
"NOR" Logical "0" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_4 (4)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	6	—	2,5,9,10	—	—	3	V_4 (4)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_4 (1)							
	—	10	—	2,5,6,9	—	—	3	V_4 (1)							
"OR" Logical "1" Output Voltage	—	5	—	2,6,9,10	—	—	3	V_5 (7)	−0.700	−0.900	−0.650	−0.825	−0.550	−0.770	Vdc
	—	6	—	2,5,9,10	—	—	3	V_5 (7)	↓	↓	↓	↓	↓	↓	↓
	—	9	—	2,5,6,10	—	—	3	V_5 (8)							
	—	10	—	2,5,6,9	—	—	3	V_5 (8)							
"OR" Logical "0" Output Voltage	—	—	5	2,6,9,10	—	—	3	V_2 (7)	−1.510	−1.880	−1.465	−1.850	−1.395	−1.790	Vdc
	—	—	6	2,5,9,10	—	—	3	V_2 (7)	↓	↓	↓	↓	↓	↓	↓
	—	—	9	2,5,6,10	—	—	3	V_2 (8)							
	—	—	10	2,5,6,9	—	—	3	V_2 (8)							
"NOR" Output Voltage Change	—	—	5	2,6,9,10	—	4②	3	ΔV_1 (4)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	—	9	2,5,6,10	—	1②	3	ΔV_1 (1)	—	−0.100	—	−0.100	—	−0.130	Volts
"OR" Output Voltage Change	—	5	—	2,6,9,10	—	7②	3	ΔV_5 (7)	—	−0.100	—	−0.100	—	−0.130	Volts
	—	9	—	2,5,6,10	—	8②	3	ΔV_5 (8)	—	−0.100	—	−0.100	—	−0.130	Volts
"NOR" Saturation Breakpoint Voltage	—	—	—	2,6,9,10	5①	—	3	V_3 (4)	—	−0.51	—	−0.55	—	−0.63	Vdc
	—	—	—	2,5,9,10	6①	—	3	V_3 (4)	—	↓	—	↓	—	↓	↓
	—	—	—	2,5,6,10	9①	—	3	V_3 (1)	—		—		—		
	—	—	—	2,5,6,9	10①	—	3	V_3 (1)	—		—		—		
Switching Times Propagation Delay Time	Pulse In	Pulse Out							Typ	Max	Typ	Max	Typ	Max	
Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	3	5	3	5	4	6	ns
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	↓	6	↓	6	↓	7	↓
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)		5		5		6	
	9	8	—	2,5,6,10	—	—	3	t_{d1} (8)		6		6		7	
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	3	6	3	6	4	7	
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	↓	5	↓	5	↓	6	
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)		6		6		7	
	9	8	—	2,5,6,10	—	—	3	t_{d2} (8)		5		5		6	
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_{d1} (4)	4	7	4	7	5	8	
	5	7	—	2,6,9,10	—	—	3	t_{d1} (7)	5	10	5	10	6	11	
	9	1	—	2,5,6,10	—	—	3	t_{d1} (1)	4	7	4	7	5	8	
	9	8	—	2,5,6,10	—	—	3	t_{d1} (8)	5	10	5	10	6	11	
	5	4	—	2,6,9,10	—	—	3	t_{d2} (4)	5	10	5	10	6	11	
	5	7	—	2,6,9,10	—	—	3	t_{d2} (7)	4	7	4	7	5	8	
	9	1	—	2,5,6,10	—	—	3	t_{d2} (1)	5	10	5	10	6	11	
	9	8	—	2,5,6,10	—	—	3	t_{d2} (8)	4	7	4	7	5	8	
Rise Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	7	4	7	5	9	
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	6	↓	6	↓	8	
	9	1	—	2,5,6,10	—	—	3	t_r (1)		7		7		9	
	9	8	—	2,5,6,10	—	—	3	t_r (8)		6		6		8	
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_r (4)	4	9	4	9	5	10	
	5	7	—	2,6,9,10	—	—	3	t_r (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_r (1)							
	9	8	—	2,5,6,10	—	—	3	t_r (8)							
Fall Time, Fan-Out = 1	5	4	—	2,6,9,10	—	—	3	t_f (4)	4	6	4	6	5	7	
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_f (1)							
	9	8	—	2,5,6,10	—	—	3	t_f (8)							
Fan-Out = 10	5	4	—	2,6,9,10	—	—	3	t_f (4)	6	11	6	11	7	12	
	5	7	—	2,6,9,10	—	—	3	t_f (7)	↓	↓	↓	↓	↓	↓	
	9	1	—	2,5,6,10	—	—	3	t_f (1)							
	9	8	—	2,5,6,10	—	—	3	t_f (8)							

Pins not listed are left open. ①Input voltage is adjusted to obtain dV "NOR" / dV_{in} = 0. ②Current test conditions: no load = 0; full load = −10 mAdc ±5%.